Pseudo-differential OTA Design with ±0.9V Wide Input Swing Range in 0.18µm Submicron Technology

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Abstract - In this paper we present a novel approach in the design of a pseudo-differential operational transconductance amplifier having a wide input range being adapted to the implementation of a 9th-order Bessel filter. Inclusion of a PMOS device biased at the subthreshold and triode regions facilitated an improvement of 40% in the input swing range by suspending half of the supply, while maintaining degradation of transconductance *Gm* to less than 1%. The operational transconductance amplifier is fabricated using a 0.18- μ m n-well 1P5M CMOS process with a 1.8V supply. Results through measurement show 1% *Gm* variation, and a total harmonic distortion of below -62dB under the input swing range of ±0.9V. The 9th order Bessel filter shows the cutoff frequency of 100MHz highly desirable for a digital versatile disc pickup circuit operating at 16 times normal speed.

I. INTRODUCTION

In the CMOS design domain, the supply voltage (*VDD*) and threshold (V_{TH}) voltage have been gradually reduced as scaling of the processing technology became more prevalent. The benefit has been a reduction in power consumption. However, V_{TH} is more difficult to reduce because of the expected increase in the leakage current. Thus, the reduction rate of *VDD* is higher than that of V_{TH} [1]-[3].

Thus, in analog circuit design for op-amps, operational transconductance amplifier (OTA), and comparators, new approaches need to be implemented in circuit techniques to expand input range. There are several methods used to extend the input swing range while maintaining a Gm constant, and hence assuring good linearity. Folded architecture as an example is more popular than cascade architecture, although it has both many poles in frequency responses and high power dissipation. The body-driven MOSFET also supports a wide input swing range that is only used in low frequency circuits because of its small Gm [4].

It should be noted that the linearity *Gm* is influenced by the processing technology. The first order drain current of CMOS

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transistor is linear. The second order terms can be canceled with a differential architecture, while the third transistor is linear. The second order terms can be canceled with a differential architecture, while the third order terms become the main source of nonlinearity. The third order nonlinearity terms can be engineered such that it can be canceled with combination of *Gms* operating in different regimes [5]. Thus, the input extension techniques of OTA become a necessary part of the design process with the advancement of the process and foundry technology. We consider not only the mobility reduction effect, but also the other second order nonideal effects for process technologies below $0.18-\mu$ m CMOS technology.

In this paper, we propose a wide input pseudo-differential OTA that provides ± 0.9 V input range keeping constant *Gm* below 0.18- μ m CMOS process with a 1.8V supply. The circuit introduces the parallel combination of a *Gm* control path at the triode and the subthreshold region transistors with the same sign of input. The proposed OTA has the advantages of wide input swing range as well as good linearity with less than 1% variation. This paper is organized as follows. Section II presents the proposed OTA's structure and properties. The OTA-C filter implementation is presented in Section III. Section IV analyzes the simulation and measurement results. The conclusions are presented in Section V.

II. THE PROPOSED OTA

A. Device characteristics in the advanced submicron process The CMOS device characteristics are partially changed as the process is advanced to a deep submicron. Fig. 1 shows the drain current and transconductance versus the gate-source voltage in the triode region MOSFET for over 0.25- μ m and under 0.18- μ m CMOS technologies, respectively. The V_{DS} is keeping the triode region 0.1V, $V_{DS} < V_{GS} - V_{TH}$. For the simulation, we tied the source of NMOS to GND and provided gate voltage, V_{GS} , up to the normal VDD level. The drain current of the NMOS transistor in the triode region starts to increase when V_{GS} is from just over V_{TH} . The slope of the drain current, Gm, rises steeply at the beginning of the triode region as shown in Fig. 1. However, Gm gradually decreases with the input increasing after it reaches the peak. In addition, the gradient of Gm (= ΔGm) tends to depend on the technology: 0.18- μ m technology has a minus sign, while

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0.25- μ m tech nology has a plus sign for the input voltage range from *VDD* to *Gm*'s peak point.

The small variation of the drain current largely affects Gm for the advanced DSM process. The kind of Gm-C filter application, moreover, requires a very wide input range, while Gm is kept flat. Fig. 2 shows a sign of gradient variation of Gm according to the technologies, while the V_{GS} decreases VDD to V_{TH} in the triode region. The Gm gradient has a minus sign under the advanced DSM technology such as under the 0.18- μ m CMOS process.

B. The Proposed wide input OTA

Fig. 3 shows the proposed pseudo-differential OTA that supports a very wide input range under 0.18- μ m technology. The transistors M1 and M2 operate in the triode region. MOSFETs operating in the triode region provide linear I_D for V_{GS} while V_{DS} is constant. The OTA using the self-regulated technique can overcome the non-ideal effect of the lateral field that decreases effective carrier mobility μ_{eff} due to the constant V_{DS} . The transistors M3 and M4 and amplifier A form a regulated-gain-control (RGC) loop that forces the drain voltage of M1 and M2 to be equal to V_{Tune} in the input. Thus, the obtained constant V_{DS} of M1 and M2 are independent of the common-mode input voltage level, and linear Gm given by $\beta V_{DS}[5]$, [6]. The tuning voltage, V_{Tune} , adjusts the OTA's Gm. However, VDS of M1 and M2 must be low enough to ensure that each input transistor remains in the triode region.

In this circuit, the input common-mode level is tightly controlled, and V_{DS} must track V_{Tune} so as to keep I_D constant. The amplifier A is composed of a single-ended differential amplifier and a level shifter. In order to achieve the gainboosting effect, the gain at the cutoff frequency has to be greater than 20dB (10V/V) [6],[7]. The Gm distortion at the triode region is changed according to the process; we have to consider adding a path for current compensation. The proposed OTA is designed to compensate the minus slope of Gm in the triode region. The Gm slope in V_{DS} from VDD to V_{TH} is a left direction change. The M13 and M14 operating in their subthreshold regions compensate for the nonlinearity of *Gm* caused by non-ideal effects from submicron processes. The parallel connection of current paths operating in the triode and the subthreshold region cancels a distortion term with their proper aspect ratio that remarkably improves linearity of Gm. The level-shifter consists of M9-M12 that forces M13 and M14 to operate in their subthreshold region. The subthreshold current is added to the current of NMOS load, M5-M8.

Fig. 4(a) shows the output current of each transistor of the proposed OTA shown in Fig. 3. In the circuit, when v_{ICM} =0.6V; v_i is decreased from -0.3V to -0.5V; differential input $v_{IP} - v_{IN}$ is decreased from -0.6V to -1V; and M2 is operated in the triode region that decreases i_{D2} . The Gm of each transistor is extremely affected by the small change of the output current as shown in Fig. 4(a). The slope of Gm_2 to the left direction in the dotted rectangular is a minus sign. The total Gm from $i_{D2} - i_{D1}$ in this region is lower than the average Gm. For the 0.35- μ m process, the input swing range extension technique is conventionally carried out by adding the subthreshold current i_{D13} to i_{D2} . In the 0.18- μ m process, on

the other hand, i_{D13} is added to i_{D1} to retain a flat Gm.

The I/V linear characteristics of the proposed OTA are shown in Fig. 5. The absolute slope of the triode current is gradually decreased in the edge of differential input swing range within 0.9V. On the other hand, the absolute slope of the subthreshold current starts to increase in the same region.



(b) CMOS process under 0.18- μ m.

Fig. 1. Transistor characteristics with various CMOS processes in the triode region ($V_{DS} = 0.1$ V).



Fig. 2. Sign of Gm slope variation according to the CMOS process.



Fig. 3. OTA with the proposed input swing range extension technique.



(a) The output current of each MOSFET.



(b) Transconductance(Gm) of each MOSFET.



Fig. 6 shows the total Gm of the proposed OTA that is expressed in

$$Total Gm = Gm_8 - Gm_7$$

= $(Gm_2 + Gm_{14}) - (Gm_1 + Gm_{13})$
= $(Gm_2 - Gm_1) + (Gm_{14} - Gm_{13})$
= Triode Gm + Subthreshold Gm
= $\frac{\Delta(i_{D8} - i_{D7})}{\Delta(\nu_{IP} - \nu_{IN})} = \frac{\Delta(i_{D2} - i_{D1})}{\Delta(\nu_{IP} - \nu_{IN})} + \frac{\Delta(i_{D14} - i_{D13})}{\Delta(\nu_{IP} - \nu_{IN})}$ (1)

As shown in Fig. 6, the triode Gm at the vicinity of the differential input ± 0.9 V is decreasing, while the subthreshold Gm at both edges is increasing. By combing these Gms, we obtain the total Gm flat expanding input range wide that is the solid line curve at the upper side in Fig. 6.

The overall Gm is 2ms for the input range of ± 0.9 V, and the Gm variations are less than 1%, that is 40% expansion of input ranges. In the proposed circuit, a higher Gm can be obtained by decreasing the tuning voltage, V_{Tune} (=larger V_{DS}), at the cost of reducing the input swing range. The practical circuits suffer from process variations and mismatch that result in a Gm fluctuation. Fig. 7 shows the transconductance variations of the proposed OTA obtained from Monte-Carlo simulations.

Mismatches of W, L, and V_{TH} are considered in the simulations. The SPICE parameters, *xln*, *xlp*, *xwn*, *xwp*, *delvton*, and *delvtop*, are randomly selected within the 3-sigma at absolute Gaussian distribution, and are applied to the transistors of the proposed OTA. The distribution of *Gm* is 1.94ms to 2.06ms (2ms \pm 3%) that the *Gm* curves show variations smaller than \pm 1%.



Fig. 5. Linearized I/V curves of the proposed OTA.



Fig. 6. Total transconductance(*Gm*) of the proposed OTA.

B. Common-mode control circuits

A disadvantage of the fully differential OTA is to require an extra common-mode feedback (CMFB) circuit to control the common-mode voltage at different nodes. The circuit can be destabilized by the negative differential feedback. To stabilize the CM circuit, we choose a reference voltage yielding the maximum differential voltage gain and output voltage swing. The poor common-mode gain leads to significant variations of OTA outputs, unless the CMFB circuit is not used. The common-mode feed forward (CMFF) circuit, however, reduces OTA gain at a low frequency [6].

The proposed pseudo-differential OTA includes CMFB and CMFF that supports CM control easy [8], [9]. The topology of this circuit is shown in Fig. 8 that is a differential difference amplifier CMFB is composed of a CM detector and a V-I converter.

The circuit compares the output common-mode voltage with V_{ref} and converts the voltage difference into current. The current is then fed into transistors MF9 and MF10 through the current mirror consisting of MB5, MB6, MB5', and MB6'. MB1, MB2, MB1', and MB2' work in the triode region since their gates are connected to GND. These transistors are a source degeneration configuration operating as resistors that improve the linearity of the CMFB.



Fig. 8. Common-mode control circuits.

III. BESSEL FILTER

We designed a 9th-order Bessel filter using a *Gm-C* element based on the proposed OTA. The filter that is shown in Fig. 9 is often used as the front-end circuit of a read channel in hard disks, CD players, and DVD players [5].



Fig. 9. 9th-order Bessel filter.

The filter consists of four biquads and a 1st-order low-pass filter (LPF). All the input and output signals are fully differential signals to accommodate common-mode noise rejection. The structure of the biquad is composed of four OTAs with the same transconductance, two fully differential amplifiers, four common-mode feedback (CMFB) circuits, four capacitors, and four transistors whose gates are controlled by V_Z . Two fully differential amplifiers provide high-speed and high-gain features that make the corner frequency of the integrator insensitive to the parasitic capacitance [5]. The Bessel filter is a good application to evaluate the proposed OTA as well as amplify a small swing in wide range input signal [10].

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IV. SIMULATION RESULT

We simulated the proposed OTA and 9th-order Bessel filter using 0.18- μ m n-well 1P5M CMOS processes under a 1.8V supply. The nominal static power consumption of OTA is 10.8mW. The evaluated the total harmonic distortion (THD) for the two kinds of OTAs are shown in Fig. 10. The proposed OTA shows lower THD below -62dB over the differential input voltage of $1.8V_{PP}$. The third-order harmonic distortion of the output currents dominates the nonlinearity of the OTA characteristics. Fig. 11 shows the filter frequency response. The cutoff frequency f_c is 100MHz. The group delay is almost constant by 10ns over f_c , and the group delay ripple is less than 10% over the range of $0.5f_c$ to $2f_c$. It can be used in an amplifier of the pick-up head for a 16x DVD with 70MHz bandwidth.







Fig. 11. Frequency response of the 9th-order Bessel filter.

IDEC Journal of Integrated Circuits and Systems, VOL 3, No.3, July 2017

Reference	[1]	[2]	[4]	[9]	[11]	This work
Technology	0.35-µm CMOS	0.35-µm CMOS	0.5 - μm CMOS	0.18-µm CMOS	0.18-µm CMOS	0.18-µm CMOS
Transconductance	90µs	870µs	1065µs	1000µs	470µs	2000µs
Linearity	-60dB THD at 100kHz	-48dB THD at 20MHz -40dB IM3 at 65MHz	-43dB THD at 30MHz	-52dB IM3 at 50MHz	-60dB IM3 at 40MHz	-62dB THD at 1MHz -43dB IM3 at 70MHz
Input swing range	$1.6V_{PP}$	2VPP	$0.9V_{PP}$	$0.4V_{PP}$	$0.9V_{PP}$	$1.8V_{PP}$
Supply voltage	3.3V	2.3V	3.3V	1V	1.5V	1.8V
Normalized input swing range	0.48	0.87	0.27	0.4	0.6	1

TABLE I. Comparison with previously-reported work



Fig. 12. Chip microphotograph of the 9th-order Bessel filter.



Fig. 13. Group delay in time domain (T=10ns to 320ns).

The chip microphotograph of the Gm-C filter is shown in Fig. 12. The capacitors are implemented utilizing an MIM structure. The active area of the filter is about $4mm^2$. The group delay at the time domain is shown in Fig. 13, in that we applied six sine waves of 0.9V over the period of 10ns, 20ns, 40ns, 80ns, 160ns, and 320ns. The crossing point of the output signals is well observed as shown in Fig. 13. As the input frequency increases to 10ns, the output becomes smaller, because the filter gain decreases toward -3dB. The limitation of the input swing range is under the supply voltage as theoretically predicted due to the departure of the correct working regions.

Table I summarizes this work. In order to compare with different implementations of OTAs, we normalized the input swing range that takes the ratio of the input swing range and supply voltage. The proposed OTA shows the widest normalized input swing range.

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V. CONCLUSION

In this paper, we proposed a new pseudo-differential OTA with an input extension technique that combines PMOS current paths operating at the triode and subthreshold regions. The circuit expands the input range by reducing the 3rd harmonic of the drain current and compensating Gm at the input range edge. The input range extension technique is modified according to the changed trend of Gm variation in the valid linear input range in DSM process. We implemented the proposed OTA using a 0.18-µm n-well 1P5M CMOS process under a 1.8V supply. The OTA shows expanding 40% of the input swing range of ± 0.9 V keeping Gm variation less than 1% and lower THD 62dB. A 9th order Bessel filter for a DVD read channel equalizer employing the proposed OTA was fabricated. The filter shows a cutoff frequency of 100MHz that can be used for a DVD pickup amplifier working at 16x.

ACKNOWLEDGMENT

This work is supported by IDEC.

REFERENCES

- E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *IEE Proc. Circuits Devices Syst.*, pp. 3-12, 2000.
- [2] K. C. Kuo and A. Leuciuc, "A linear MOS transconductor using source degeneration and adaptive biasing," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 48, no. 10, pp. 937-943, Oct. 2001.
- [3] M. Mobarak, M. Onabajo, J. Silva-Martinez, and E. Sanchez-Sinencio, "Attenuation-predistortion

linearization of CMOS OTAs with digital correction of process variations OTA-C filter applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 2, pp. 351-367, Feb. 2010.

- [4] X. Zhang and Ezz. I. El-Masry, "A novel CMOS OTA based on bodydriven MOSFETs and its applications in OTA-C filters," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 6, pp. 1204-1212, June 2007.
- [5] S.-H. Yang, K.-H. Kim, Y.-H. Kim, Y. You, and K.-R. Cho, "A novel CMOS operational transconductance amplifier based on a mobility compensation technique," *IEEE Trans. Circuits Syst. II*, vol. 52, no. 1, pp.3742, Jan. 2005.
- [6] C. Mingdeng, J. Silva-Martinez, S. Rokhsaz, and M. Robinson, "A 2VPP 80-200-MHz fourth-order continuous-time linear phase filter with automatic frequency tuning," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1745-1749, Oct. 2003.
- [7] A. Kranti and G. Alastair Armstrong, "Nonclassical channel design in MOSFETs for improving OTA gainbandwidth trade-off," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 12, pp. 3048-3054, Dec. 2010.
- [8] A. N. Mohieldin, E. Sanchez-Sinencio, and J. Silva-Martinez, "A fully balanced pseudo-differential OTA with common-mode feedforward and inherent common-mode feedback detector," *IEEE J. Solid-State Circuits*, vol. 38, no. 4, pp.663-668, Apr. 2003.
- [9] F. Rezzi, A. Baschirotto, and R. Castello, "A 3V pseudodifferential transconductor with intrinsic rejection of the common-mode input signal," *in Proc. Circuits and Systems*, pp. 85-88, 1994.
- [10] Siva V. Thyagarajan, S. Pavan and P. Sankar,"Active-RC Filters Using the Gm-Assisted OTA-RC Technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1522-1533, Jul. 2011.
- [11] T. Y. Lo and C. C. Hung, "A high speed and high linearity OTA in 1-V power supply voltage," *in Proc. ISCAS 2006*, pp. 1834-1867, 2006.
- [12] T. Y. Lo and C. C. Hung, "A 1-V 50-MHz pseudodifferential OTA with compensation of the mobility reduction," *IEEE Trans. Circuits Syst. II*, vol. 54, no. 12, pp. 1047-1051, Dec. 2007.
- [13] T. Y. Lo and C. C. Hung, "A 40-MHz double differential-pair CMOS OTA with -60-dB IM3," *IEEE Trans, Circtuis Syst. I*, vol. 55, no. 1, pp. 258-265, Feb. 2008.
- [14] O. Abdelfattah, G. W. Roberts, I. Shih, and Y. C. Shih, "An ultra-low-voltage CMOS process-insensitive selfbiased OTA with rail-to-rail input range." *IEEE Trans. on Circuits Syst. I*, vol. 62, no.10, pp. 2380-2390, 2015.
- [15] A. P. Nicholson, A. Iberzanov, J. Jenkins, T. J. Hamilton, and T. Lehmann, "A statistical design approach for a digitally programmable mismatch-tolerant highspeed Nauta structure differential OTA in 65-nm CMOS." *IEEE Trans. on VLSI Systems*, vol. 24, no. 9, pp. 2899-2910, 2016.



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