16 channel ultralow power analog front-end for an implantable neural recording microsystem

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***Abstract* - Recording neural signal is fundamental in the neuroscience research as well as in the neural prosthetic systems enabling the treatment of neurological diseases and the restoration of sensory and motor disabilities. For these purposes, researches on neural interface connecting the nervous system to external device have been developed for several decades. Especially, multi-channel neural interfacing microsystem has been developed by using semiconductor process. However, current integrated circuit system has unacceptable noise level and requires a lot of power consumption to be implanted. Besides, there is no permanent power source and the battery has to be changed when it discharges which causes danger for infection. In order to solve these problems, many researchers have divided the whole system into outer, inner part and supply power wirelessly by inductive coupling. To have the circuit in function with limited amount of power, an inner part of brain recording system is needed to achieve maximum efficiency as neural recording system consumes the most power in the whole inner circuit system. Our proposing neural recording system which is built in a standard 0.18um CMOS technology can amplify neural signal such as local field potential and action potential with programmable gain from 52-60dB with very low power consumption. The input referred noise of low noise amplifier is 8uVrms in the spike recording settings and 6uVrms for local field potential. The 8bit SARADC is connected to output of recording system and digitize each signal with sampling rate of 20kS/s per channel. After digitized, output signals are transmitted to cross-coupled complementary voltage controlled oscillator to use binary frequency shift keying for wireless communication. Our system has two different supply voltages that are 1V for analog part and 1.8V for digital part. Total recording system consumes below 1mW power.**

I. INTRODUCTION

Humans have brains that control all actions and thougths, functioning as a central processing unit of the body[1]. The brain signal spontaneously released when humans do such actions and thoughts is able to be analyzed and this has been in spotlight for many scientists. Brain-Machine-Interface is outstanding in that it allows patients who have their brain neuronal system damaged to move their wheel chair by oneself just by thinking. This is possible because our neuronal system has their information transferred by electrical signals. Current BMI systems are based on non-invasive methods to help disabled with their rehabilitation. However, limits exist such as difficulties to obtain specific brain signals from a complicated potential that has been normalized, highly vulnerable to noise, and misinterpretations when analyzing local brain activities due to diffraction, diffusion and attenuations of brain signals.

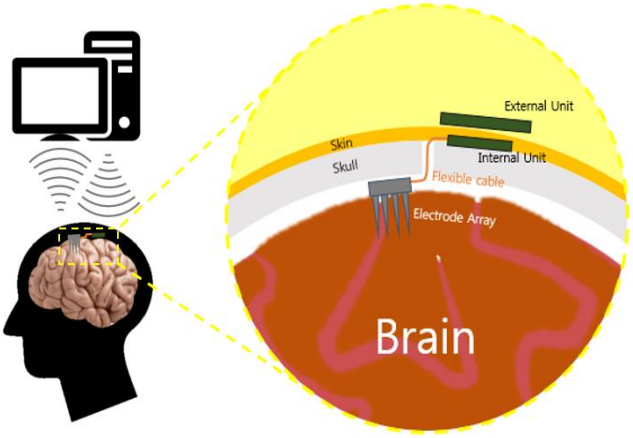

Fig. 1. Conceptual diagram of Brain Machine Interface.

Practically, the development of invasive BMI (Brain Machine Interface) allows paralyzed patients to control external device or compensate damaged vision of visually impaired people. Invasive recording method is a technique that utilized microelectrode array surgically implanted in gray matter to achieve high signal-to-noise ratio and spatial resolution. However, surgical insertion of microelectrode array can cause neurological damage and transcutaneous connection between electrode and external device raise the risks of infection.

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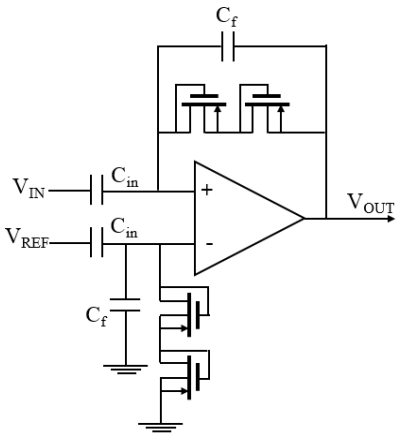

Fig. 2. Schematic of capacitive-feedback neural amplifier.

Ultralow power consumption is pursued so that the results of this study would be used for pre-clinical and clinical applications with wireless power transfer system. Present popular devices, depicted in Fig. 1, consist of multi-electrode array using capacitive feedback network as shown in Fig. 2[2]. The midband gain is determined by ratio of the input and feedback capacitance and dc offset voltage from electrode-tissue interface can be removed by closed-loop DC suppression schemes which is proper for neural recording system. In this paper, we suggest ultralow power neural signal recording system which are appropriate to be inserted in brain.

II. FUNCTIONAL BLOCK OF SYSTEM

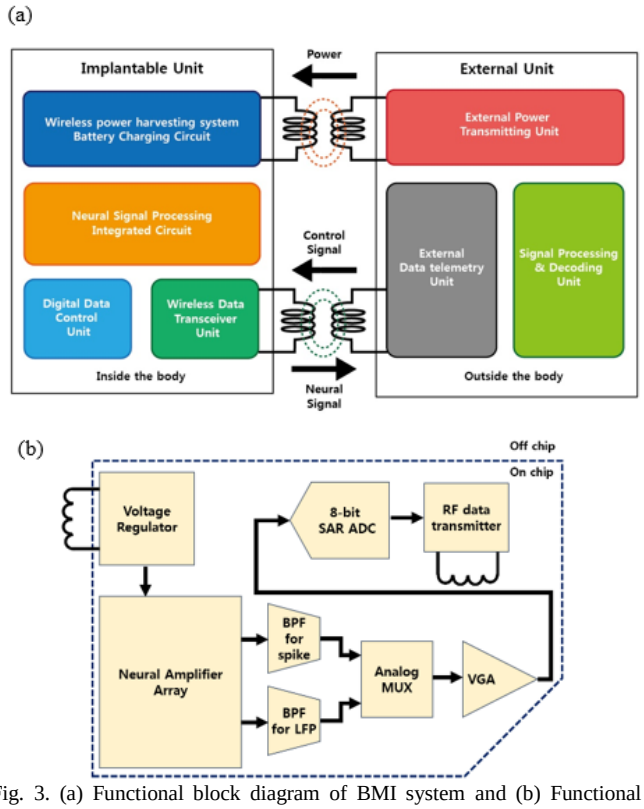

Fig. 3. (a) Functional block diagram of BMI system and (b) Functional block diagram of front-end neural signal processing IC.

Fig. 3. shows the block diagram of BMI full system and inner part of recording module. We designed front-end neural recording IC which consisted of analog part and digital part.

A. Neural Signal Processing IC

Bio-amplifier can amplify neural signal which transmitted through the microelectrode array with acceptable noise level. Generally, noise level of system is determined by front-end amplifier. So, more attention is needed to design low noise amplifier. This block contains neural amplifier, band pass filter and variable gain amplifier.

B. Digital Data Control Unit

The function of digital data control unit is to convert analog signal which amplified by LNA to digital signal and control the amount of data. This block controls the automatically programmable gain and configure data such as total gain, type of brain signal and which channel is monitored.

C. Wireless Data Transceiver Unit

Data telemetry unit delivers the data to outside of chip by using inductive link or RF data communication. Most of reported papers used ASK or FSK technique. In FSK, two carrier frequencies have same amplitude. FSK has the advantages that transmit constant maximum power to transmitting and receiving system through wireless inductive link. In ASK, if all parameters are constant except distance the voltage induced in receiving coil is inverse proportion to the cube of the distance. This is a drawback to the ASK system for communicating information and not suitable for moving patient. On the other hand, FSK systems do not significantly affected by transmission distance or a change of induced current, which is a proper technique for bio-implant system.

D. External Power Transmitting Unit

Power to drive neural recording system can be received from outside inductive coil. It is often used low frequency band powering system by magnetic fields but this system has some limitations due to its distance and alignment between coils.

III. EXPERIMENTS

A. Low Noise Amplifier

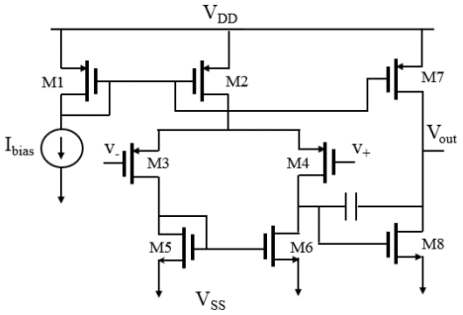

Fig. 4. Schematic of low noise amplifier

In Fig. 4. the schematic of the proposed two stage neural recording amplifier is shown. The first stage consists of differential pair and current mirror load by M5, M6. In particular, it is critical that input pair transistors(M3, M4) should have highest value of transconductance to reduce noise level. The second stage which consists of a common source transistor M8 and the current source load compensates ac response of amplifier. Regardless of the amount of negative feedback, the amplifier is to operate stably without oscillation. To stabilize a frequency characteristics, the pole which exist in relatively low frequency must be major role of determining the ac response. In this structure, the compensating capacitor C_c is inserted in negative feedback path of the second stage amplifier. Each transistor operates in weak, moderate or strong inversion regions[3] and this topology is proper to drive capacitive loads and to reduce input reffered noise.

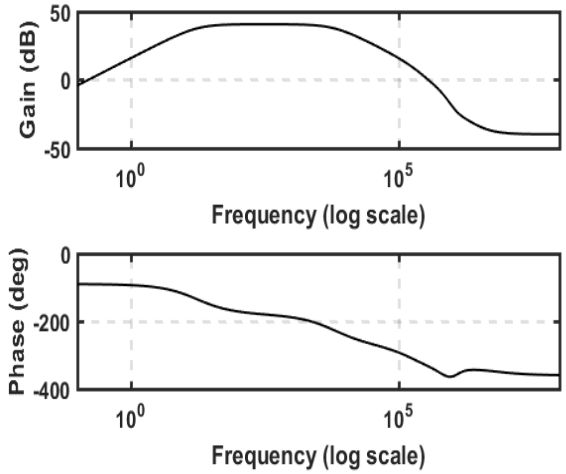

Fig. 5. Simulated transfer function of low noise amplifier.

Fig. 5 shows the simulated ac response of low noise amplifier. The midband gain is 40.7dB and low cut off frequency is 10Hz by pseudo resistor.

Table I. presents the simulated performance of low noise amplifier.

TABLE I
Performance of LNA

Supply voltage	1V
Power	5.5uW
Gain	40.7dB
Input-referred noise	AP : 8uV$_{rms}$ LFP : 6uV$_{rms}$
Bandwidth	10Hz ~ 6.1kHz
CMRR	≥60dB
PSRR	≥60dB
Phase margin	58°

B. Gm-C filter

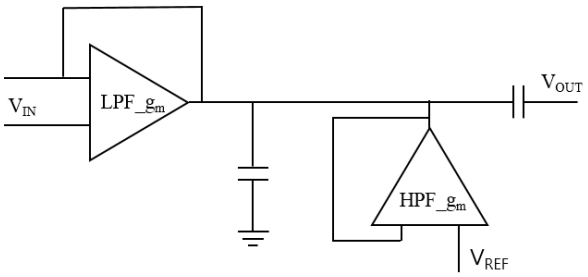

Fig. 6. Schematic of Gm-C filter.

Typical local field potential contains energy below sub hertz. Some existing neural recording systems have off chip capacitor or resister to obtain low cut off frequency to record local field potential. This method is not suitable for multi-channel acquisition system in the way that it has too large chip area. To minimize chip area we designed Gm-C filter as shown in Fig. 6. Despite the use of passive component, we designed active band pass filter that consists of classical OTA-C structure. In order to reduce noise level, it is necessary to have pole at low frequency band. Several OTA topologies have been designed to have very small transconductance and wide linear range. However, existing complex OTA structures have unacceptable noise level and mismatch offset. In this work, we use very low transconductance OTA in the pico siemens range by using series-parallel division of current method[4][5] as shown in Fig. 7.

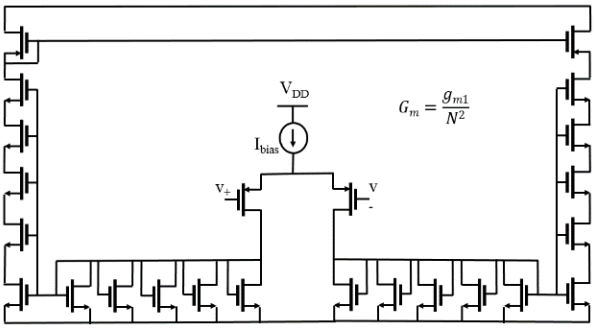

Fig. 7. OTA with SP current division.

Placing unit transistor in series and parallel, the output transconductance G_m is minimized.

$$G_m = \frac{g_{m1}}{N^2}$$

where N is number of unit transistor, and gm1 is the gate transconductance of input pair.

Both spikes and local field potential can be recorded by changing bias current. The simulation results are shown in Fig. 8. During recording action potential and local field potential, Gm-C filter consumes 2.2uW and 2uW of power, respectiviely.

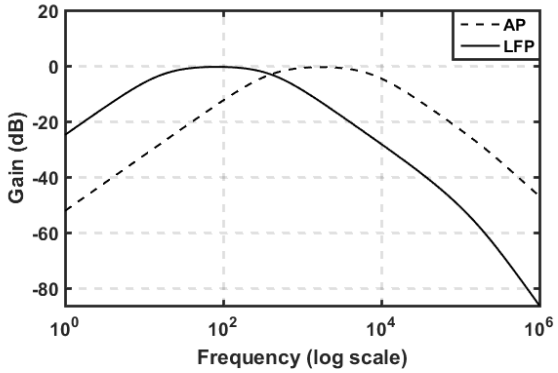

Fig. 8. Magnitude response of the Gm-C filter at different neural signal.

Table II. presents bandwidth of Gm-C filter for local field potential and action potential.

TABLE II.
Bandwidth of Gm-C filter when selection signal is high or low

Local field potential	12Hz ~ 330Hz
Action potential	350Hz ~ 7kHz

C. Analog multiplexer

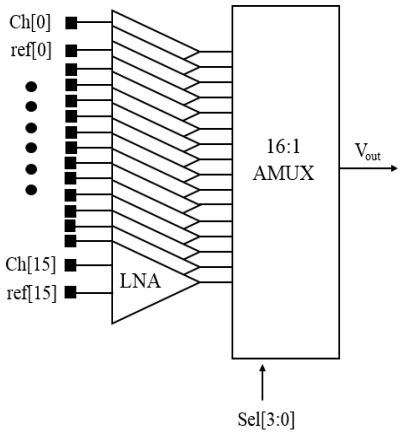

Fig. 9. Simplified block diagram 16:1 multiplexer.

A 16 channel analog multiplexer using complementary analog shunt switch topology is shown in Fig. 9. The outputs of 16 low noise amplifiers are connected to analog multiplexer and transmitted to variable gain amplifier in recording module. Amplifier′s output signals are multiplexed by the selection signals S0-S3. Because gain of low noise amplifier is enough to attenuate the noise of multiplexer, the input referred noise of analog multiplexer is not important.

Fig. 10. shows transient response of analog multiplexer.

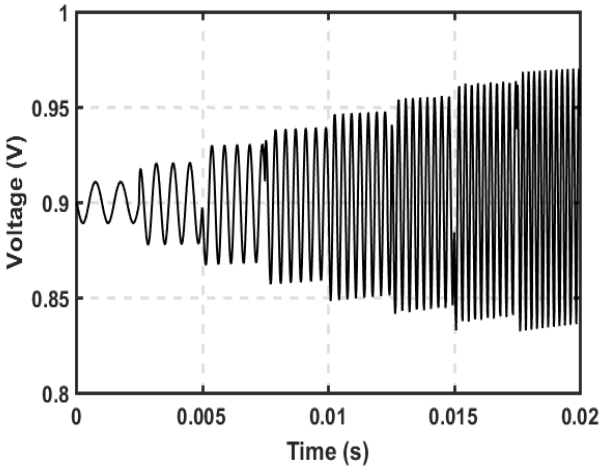

Fig. 10. Transient response of analog multiplexer.

D. Programmable gain amplifier

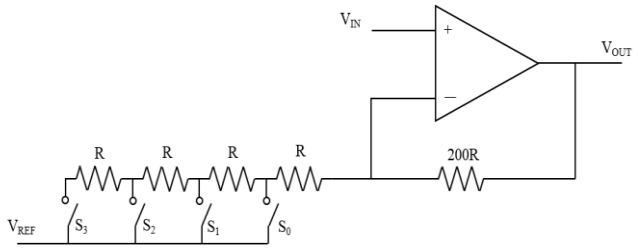

Fig. 11. Schematic of programmable gain amplifier.

After multiplexed, signal is transmitted to the programmable gain amplifier in Fig. 11 which amplifies the signal that range from 12dB to 20dB by control signals S0-S3. As a result, whole gain of analog recording module is from 52dB to 60dB which is appropriate for output voltage swing range considering the input voltage.

Changing the input voltage of analog decoder D1 and D0, the gain of programmable amplifier is varied as tabulated in Table Ⅲ. Total power consumption of programmable gain amplifier is 3uW.

TABLE Ⅲ.
Gains of the programmable gain amplifier

Switch	**D_1**	**D_0**	**Gain (dB)**
S_0	0	0	12
S_1	0	1	15
S_2	1	0	18
S_3	1	1	20

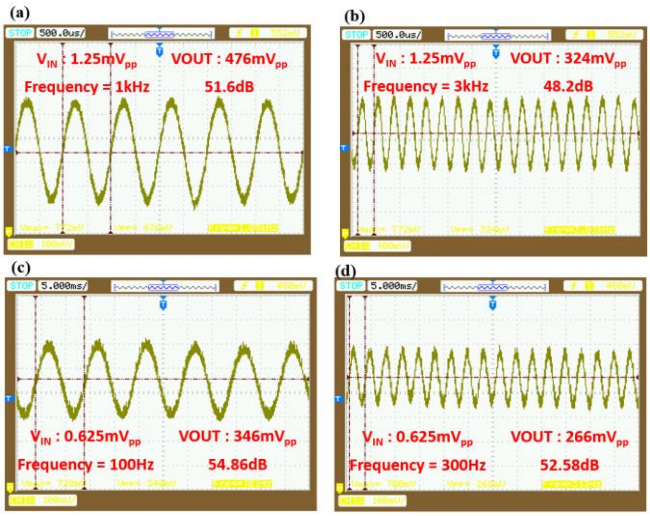

Fig. 12. Tested result when applying sinusoidal signal of action potential frequency band (a)1kHz, (b)3kHz and local field potential frequency band (c)100Hz, (d)300Hz.

Fig. 12. shows the measured sinusoidal response of the amplifying module that consists of low noise amplifier and programmable amplifier. When applying input voltage of analog decoder close to S0, we are confirmed that the total gain of recording module is 51.6dB at 1kHz and 48.2dB at 3kHz respectively as shown in Fig. 13(a)(b). This discrepancy is caused by pseudo resistor because its bias point is not stable. Also, we identify magnitude of recording module when it is close to S1 switch as shown in Fig.13(c)(d).

E. LC VCO

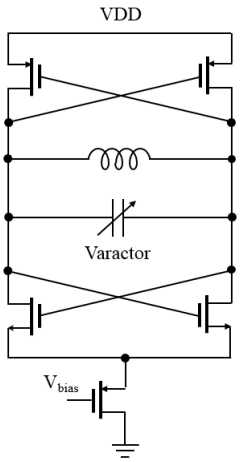

Fig. 13. Schematic of cross-coupled complementary LC VCO.

A voltage controlled oscillator is designed for modulating the data from ADC using binary frequency shift keying(BFSK)[6]. Due to relatively low phase noise response and low power consumption, cross-coupled complementary topology is chosen consisting of two blocks of cross coupled nMOS and pMOS current source pair as shown in Fig. 13. Oscillation frequency or working frequency is determined by external voltage Vcon. In this work the oscillation frequency changes by applying different input voltages of varactor(a variable capacitor); it modifies capacitance of varactor.

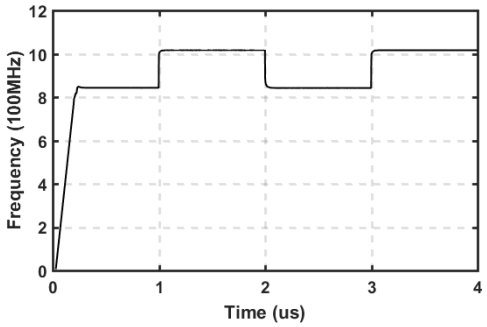

Fig. 14. Transient frequency response of LCVCO high and low voltage.

The measurement of the working frequency versus input voltage of varactor is shown in Fig. 14. In this design, parameter of phase noise and KVCO are not important since we just transmit the signal only high and low. Table IV. summarizes the performance of LC-VCO.

TABLE IV.
Performance of VCO

Parameter	Value
High	1.01GHz
Low	846MHz
Power	580uW
Setup time	300ns

F. SARADC

Analog to Digital Converters are important block such as implantable systems since it requires a lot of power consumption. Because the bandwidth of neural recording amplifier is below 5kHz, we choose sampling frequency per channel in the spike recording at 20kHz which is slightly higher than Nyquist frequency. Successive approximation register(SAR) logic is designed by 8bit because it has good energy efficiency and sufficient resolution under 1.8V supply voltage.

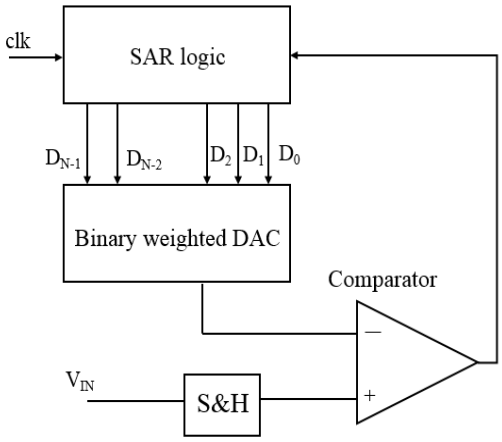

Fig. 15. Functional block diagram of SARADC.

The sample and hold circuit, comparator, successive approximation register and binary weighted capacitor are main components of SARADC as shown in Fig. 15.

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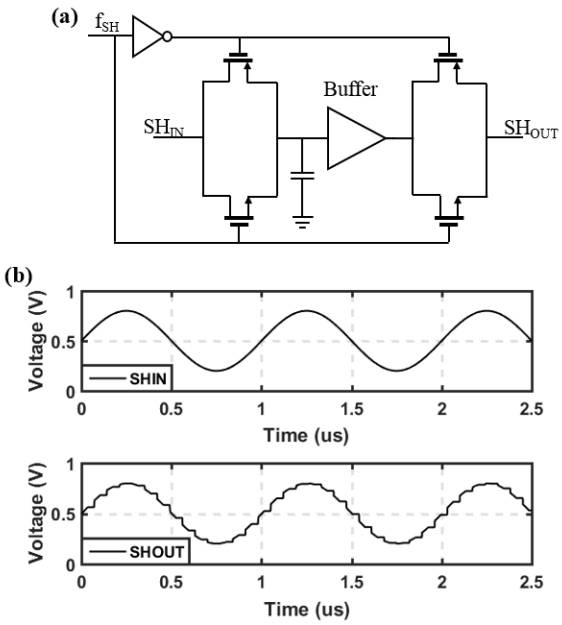

Fig. 16. (a) Schematic of sample and hold circuit and (b) simulation result of sample and hold mode.

To connect or disconnect from the input signal, the sample and hold circuit uses capacitor, an analog switch and buffer as shown if Fig. 16(a). In sampling mode, depicted in Fig. 16(b), the analog switch is ′on′ and capacitor is charged to track input signal. When hold mode, analog switch is opened and the capacitor is disconnected from input signal. The time interval from sample mode to hold mode is called sampling frequency $f_{S\&H}$.

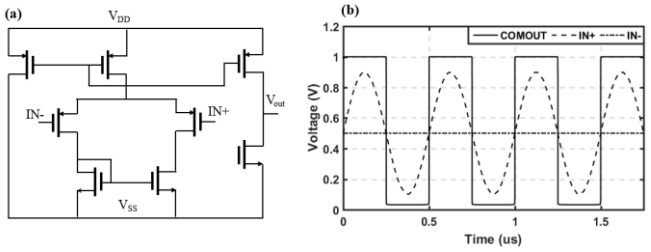

Fig. 17. (a) Schematic of comparator and (b) simulation result when applying sinusoidal wave.

A comparator as present in Fig. 17(a)[7] determines a high or low logic voltage depending on a comparison of the sample and hold voltage with reference voltage generated by DAC. Since it consumes bigger power than other block, comparator needs more attention to minimize power consumption.

In addition, because the small offset voltage of comparator is unable to transmit the accurate information to the SAR logic, it is important to eliminate dc offset voltage of comparator in design.

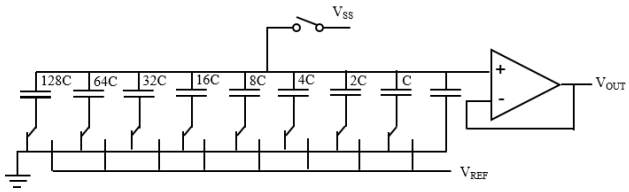

Fig. 18. Layout of digital logic of SARADC.

The binary weighted capacitor array is shown in Fig. 18. We choose unit capacitance with 44fF considering chip area and parasitic capacitor.

IV. CONCLUSIONS

TABLE V
Comparison other neural recording systems

	Rahul Sarpeshkar TBCAS '11[3]	**Georges Gielen TBCAS '12[8]**	**This work**
Supply voltage	1.8 V / 1V	3.3V	1V/1.8V
Average Power/Channel	10.1uW	11.5uW	6uW
Gain	49 - 66 dB	40 - 75 dB	52 – 60 dB
Bandwidth	0.1Hz-12 kHz	0.23Hz-6.2kHz	20Hz-5kHz
Input-referred noise	5.4–11.2 μVrms	2.3–2.9 μVrms	6-8 μVrms
Channel count	32	16	16
Chip area	4.41mm^2	16.81 mm^2	7.22 mm^2

Table V. compares our recording system to some other group′s design that achieves ultralow power consumption and low noise front-end system. The design [3] has lowest cut off frequency and robust from noise which is more proper to record local field potential. Since the design [8] is fabricated by 0.35um CMOS process, it is relatively larger than other designs considering channel count.

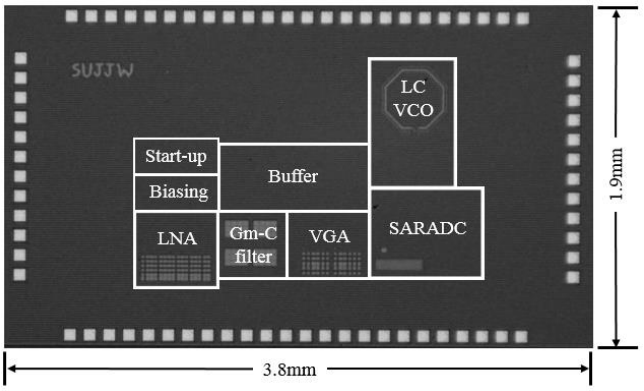

Fig. 19. Layout of MS1501.

This paper proposes a low power 16 channel neuronal activity monitoring system. Our full system can amplify neural signal such as action potential and local field

potential, digitized by 8 bit SARADC, and enable wireless telemetry. The chip photography of 16 channels neural signal recording system is shown in Fig. 19. Dimension of total chip is unable to optimize since we need I/O pads for testing. Excluding I/O pads, full chip area is 1.7mm x 1.3mm. This chip is fabricated with Magnachip/SKhynix 0.18μm technology and tested through chip on bonding (COB) process.

ACKNOWLEDGMENT

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His research interests include basic and applied semiconductor optoelectronics, such as vertical cavity lasers and nanostructured light emitters.