An IEEE 802.15.4g SUN Compliant MR-OFDM RF CMOS Transceiver for Smart Grid and CEs

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Abstract - This paper proposes an IEEE 802.15.4g SUN (Smart Utility Network) OFDM-based 920 MHz RF CMOS transceiver. It can be adopted in energy saving intelligent green homes, which are related to Smart Grid, as well as universal remote controller, building automation, which is related to CEs (Consumer Electronics), and other areas. With the proposed SUN OFDM-based RF transceiver, wireless connectivity among CE devices or among electric metering systems can considerably save electronic energy and make our lives more comfortable. The proposed RF transceiver consists of a RF front-end with an on-chip RF switch, a Tx BBA (Baseband Analog), a Rx BBA, and a PLL. The proposed RF transceiver is implemented in 0.18-μm CMOS technology and consumes 37 mA in Tx mode and 38 mA in Rx mode from a 1.8 V supply voltage. With the fabricated RF transceiver chip, two successful public demonstrations have been carried out, which show the possibility of its use in commercial products.

I. INTRODUCTION

Remote-metering of water, electricity, gas, etc. is currently performed by manual or semi-manual operation. Considering service efficiency and cost effectiveness, utility service providers accordingly require more intelligent metering systems. Radio Frequency (RF)-based mesh networking systems are a good candidate in this regard and have huge market potential in the field of metering systems. Zigbee [1], [2] is one of the solutions for RF-based mesh networking, but it has several drawbacks, including limited communication range, low data-rates, instability of mesh routing, and shadow zone problems.

To overcome these problems, the IEEE 802.15.4g SUN (Smart Utility Networks) standard was developed [3]. Because the SUN system can communicate up to several-hundred meters with a data-rate of 800 kbps and also assure reliable mesh routing, it is expected to provide a good solution for RF-base mesh networking. SUN is conceptually illustrated in Fig. 1 and its standardization has been processed in the IEEE 802.15.4g working group.

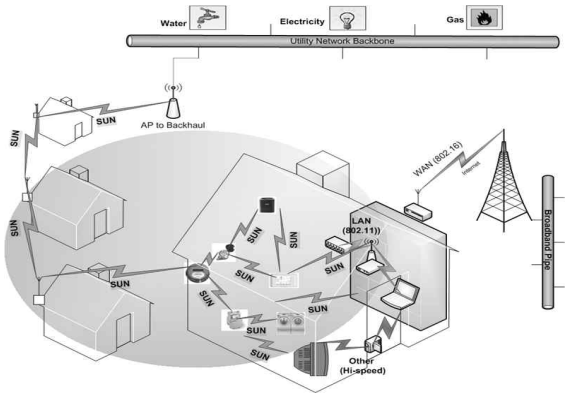

Fig. 1. SUN conceptual diagram.

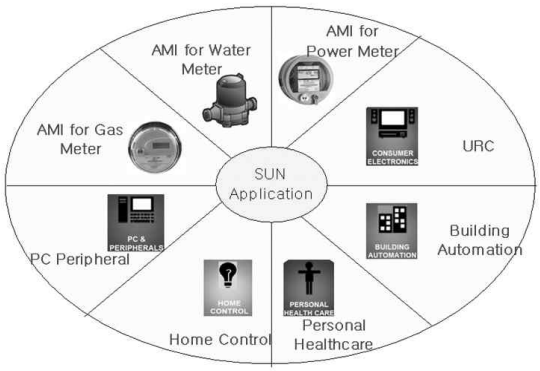

Fig. 2. SUN applications.

Advanced metering infrastructures (AMIs) for gas, water, and power metering will be a good application of SUN systems. It can also be used for PC peripherals, personal healthcare, URC (Universal Remote Control), and home control [4], [5], as shown in Fig. 2. The SUN system needs two kinds of system, a low data-rate system with very low DC power by adopting a frequency shift keying (FSK) and a high data-rate and highly stable system using orthogonal frequency division multiple access (OFDM) [3]. This paper describes a 920 MHz SUN OFDM-based CMOS RF transceiver. Section II provides a brief overview of SUN OFDM systems, and section III describes system-level simulation results to achieve design parameters of

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the RF transceiver. The RF transceiver architecture and circuit design are shown in section IV and V, respectively. Measurement results of the fabricated RF transceiver are summarized in section VI and two public demonstrations are also described in section VII.

II. System overview

Table I summaries the IEEE 802.15.4g SUN OFDM PHY specifications [3]. As can be seen in ranging from 50 kbps to 800 kbps. The subcarrier spacing is constant and is equal to 10.416 kHz. This PHY includes four options, each being characterized by the number of active tones. In Table I, the OFDM PHY supports data rates channel bandwidth, the sensitivity level, and data-rates. Thus, the total signal bandwidth for each option ranges from 1.2 MHz to 200 kHz according to the number of active tones. All devices supporting a particular option (1, 2, 3, or 4) should support all BPSK and QPSK modulation, but all 16-QAM are optional [3]. In addition, to support all options, where the channel bandwidth is different for each option, multi-channel selection filters should be used in the RF transceiver. In the receiver, when the minimum input levels with pack-error-rate (PER) of less than 10% are measured at the antenna connector, the overall receiver noise figure (NF) is specified as 10 dB, but 6 dB implementation margins are assumed [3]. This low NF is stricter than those of other WPAN standards such as Zigbee [1], [2]. The transmitter should provide a high transmitted power for wireless link of several-hundred meters. However, due to the peak-to-average power ratio (PAPR) of 10 dB in the OFDM PHY, the average transmitting power level may be about −3 dBm under a limited supply voltage (of 1.8 V).

TABLE I.
Summary of the IEEE 802.15.4g SUN OFDM spec.

	Opt. 1	Opt. 2	Opt. 3	Opt. 4
BW(KHz)	1200	800	400	200
FFT (tones)	128	64	32	16
Active (tones)	104	52	26	14
Pilot(tones)	8	4	2	2
data(tones)	96	48	24	12
DC null (tones)	1	1	1	1
Sub-Carrier. BW(kHz)	10.416	10.416	10.416	10.416
Data rates (kbps)	100 ~ 800	50 ~ 800	50 ~ 600	50 ~ 300
NF (dB)	10	10	10	10
Sensitivity (dBm), PER < 10%	-103 @100kbps	-105 @50kbps	-105 @50kbps	-105 @50kbps
Rx Max input (dBm)	-20	-20	-20	-20
Tx average Power(dBm)	>-3	>-3	>-3	>-3
Tx EVM (dB)	-10	-10 ~ -16	-10 ~ -19	-10 ~ -19

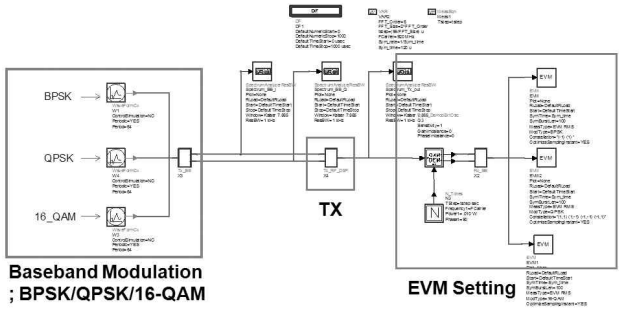

Fig. 3. Test bench of Tx RF.

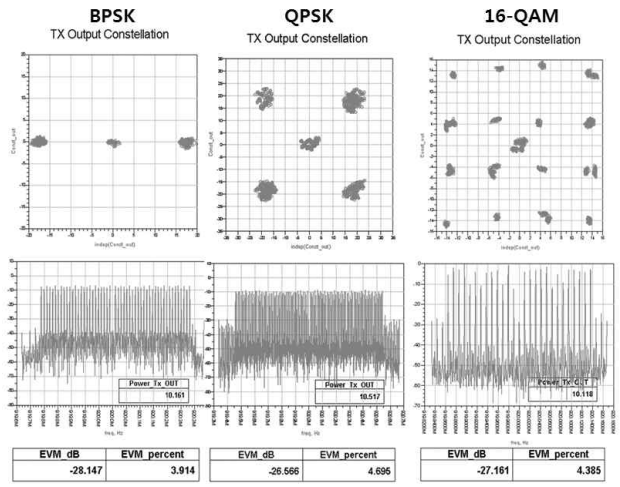

Fig. 4. Simulated Tx IQ constellations and EVMs for option2.

Furthermore, it is still difficult to achieve this kind of power level in an on-chip solution without a power-hungry power amplifier.

III. Transceiver specification

A. Transmitter

Since the carrier leakage at the transmitter output degrades the error vector magnitude (EVM) of the transmitted power, large carrier leakage should be minimized. To reduce carrier leakage, the Tx baseband circuits such as a low-pass filter (LPF) and variable gain amplifier (VGA) should be implemented as the differential topology, and a DCoffset cancellation block should be utilized. Considering the required PAPR of 10 dB in the OFDM-based transmitter, all RF and analog circuits should operate at a backoff of +10 dB from their 1-dB output compression point. To define design specifications for the RF transmitter, a system-level simulation has been processed, as shown in Fig. 3.

TABLE II.
Transmitter target specifications.

Tx Power (ave.)	> -3 ~ +0 dBm
1-db Compression Point	+7 ~ +10 dBm
Tx EVM	> -25 dB
IQ Mismatch (gain and phase)	< 0.7 dB and < 5°
Phase Noise	-114 dBc/Hz @ 1-MHz
Carrier leakage	> 15 dBc

Based on Table I, baseband modulation sources (BPSK, QPSK, and 16-QAM) compliant with the OFDM PHY have been developed in this work. In Fig. 3, the Tx block is a direct up-conversion architecture, which consists of a Tx LPF, a Tx VGA, an up-conversion mixer, a driver amplifier (DA), a T/Rx switch, and a band-pass-filter (BPF). The required phase noise of the phase-lock loop (PLL)-voltage-controlled oscillator (VCO) is calculated as -114 dBc/Hz at 1 MHz offset. Fig. 4 shows simulated IQ constellations and EVMs for option 2, which have been obtained after optimizing each circuit block's design parameters (voltage gain, linearity, input and output impedances, phase noise, and so on). Simulated Tx EVMs for all options are more than -25 dB, which is better than the required EVM of -19 dB [3]. Table II summarizes the required design parameters for the OFDM-based RF transmitter with EVMs of more than -25 dB for all options. However, after chip implementation, measured Tx EVMs will be degraded due to unexpected mismatches, process variations, and so on.

B. Receiver

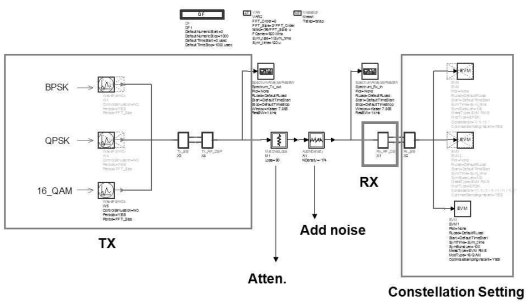

Fig. 5. Test bench of Rx RF.

TABLE III.
Receiver target specifications.

Minimum Sensitivity level	-105 dBm@50kbps (PER < 5%) -103 dBm@100kbps (PER < 5%)
Noise Figure	< 5 dB
IQ Mismatch (gain and phase)	< 0.7 dB and < 5°
Input P1db	> -20 dBm
Phase Noise	-114 dBc/Hz @ 1-MHz
Voltage gain	100 dB
Dynamic range	85 dB

To detect the minimum input signal of -105 dBm, the total voltage gain of 100 dB is needed for a fixed differential output voltage swing of 1.4 V_{pp} in this work. When the receiver accommodates the maximum input of -20 dBm, the low noise amplifier (LNA) should work in low gain mode first so as not to saturate the receiver output. Therefore, the required dynamic range of the receive is 85 dB. Since the OFDM PHY standard allocates a single DC null tone with a bandwidth of 10.414 kHz in Table I, the down-converted baseband signals in the receiver have occupied from 5.208 kHz. Therefore, the receiver can adopt a zero-IF architecture for high integration. However, low frequency noise (i.e., 1/f noise) and DC offset problems should be solved by circuit techniques.

To achieve the required sensitivity levels in Table I, a Rx system-level simulation has been also processed, as shown in Fig. 5, where modulated RF signals are generated from the designed transmitter in Fig 3. In Fig. 5, the zero-IF Rx consists of a T/Rx switch, a BPF, a LNA, a down-conversion mixer, a LPF, a VGA, and a PLL. The phase noise of -114 dBc/Hz at 1-MHz offset is also adopted in the PLL. After optimizing 98each block's design parameters, the simulated Rx EVMs at the receiver output for the RF input signals from -105 dBm to -20 dBm are more than -20 dB. Table III summarizes the receiver design parameters to achieve minimum sensitivity levels described in Table I.

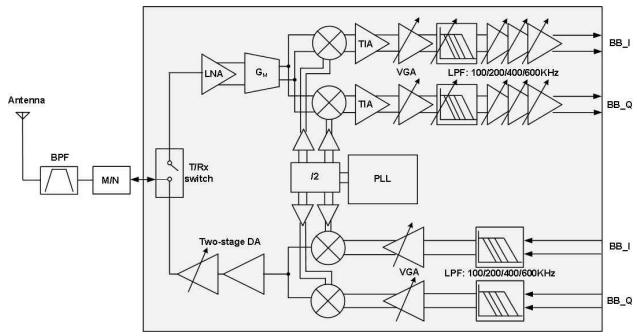

Fig. 6. Simplified block diagram of proposed zero-IF RF transceiver.

IV. TRANSCEIVER ARCHITECTURE

Fig. 6 shows a block diagram of the proposed 900 MHz OFDM-based CMOS RF transceiver. To eliminate the need for image filtering which increases the complexity and cost of the receiver, a zero-IF architecture is used in this work.

As shown in Fig. 6, the proposed RF transceiver is composed of a RF front end, a Rx baseband low-pass filter (LPF) and a variable gain amplifier (VGA), a Tx LPF and VGA, a T/Rx switch, and a VCO-PLL block.

In the proposed RF front-end, a T/Rx switch is integrated only at the input of the low-noise amplifier (LNA) so that the driver amplifier (DA)

does not experience any signal loss caused by the T/Rx switch and provides a high output power to the antenna with a high dc efficiency. An external matching network (M/N) is used commonly as an input-matching circuit for the LNA in Rx mode and an output-power matching circuit for the DA in Tx mode, resulting in a small chip area due to fewer passive components. The RF transceiver integrates a $\Delta\Sigma$ fractional-N frequency synthesizer with a complementary differential VCO running at twice the LO frequency of 1.4-to-2 GHz. A divider-by-two circuit following the VCO generates quadrature 50 % duty-cycle LO clocks for up- and down-conversion mixers. In the transmit path, quadrature analog-baseband signals are applied to a highly linear 5th-order active-RC LPF followed by a VGA. For the IQ modulation and frequency up-conversion, a single-ended quadrature voltage-mode passive mixer is utilized, which provides a high linearity with no LO leakage in the transmit path. To reduce dc power consumption, the two-stage DA has been designed with a single-ended topology, and it comprises class A and class AB amplifiers. In simulation, the transmitter achieves the output 1 dB compression point of 10 dBm with a 1.8 V supply voltage. In the receiver chain, a noise-cancelling LNA topology [6] is used. The LNA's single-ended input is connected to the output of the DA to share the matching network, and its differential output provides an active balun function for further differential signaling in the following receiver blocks. The RF signal amplified by the LNA is converted to RF current signal by a transconductance stage (G_M). Then, the RF current signal is down-converted to zero-IF by a current-driven quadrature passive mixer. To provide a large voltage swing of 1.4 V_{PP} to the analog-to-digital converter (ADC), the receiver analog-baseband circuit, comprised of a four-stage VGA and a 5th-order active-RC LPF, provides 70 dB of voltage gain with 1 dB gain control step.

V. Circuit design

Fig. 7 shows the proposed RF front-end configuration, which consists of a single-ended 2nd-stage DA (M_1 and M_2), a noise-cancelling LNA (M_G and M_S), a T/Rx switch (sw0 and sw1), and an external M/N (L_1, L_S, and C_1). As shown in Fig. 7, the single-ended DA is implemented using n-MOS transistors to provide high output power, while the noise-cancelling LNA is implemented using p-MOS transistors to connect its single-ended input to the DA's output with dc-coupling through sw0.

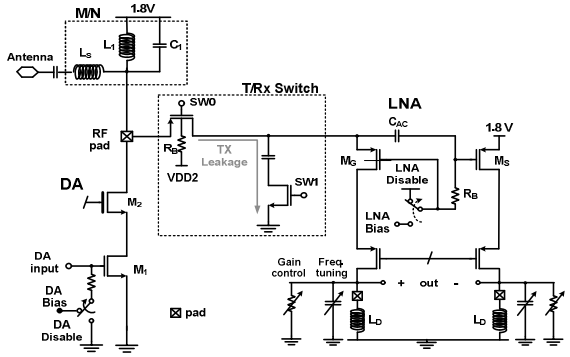

Fig. 7. Configuration of DA, LNA and T/R switches.

This configuration allows the DA and LNA to share a common RF pad and M/N. As shown in Fig. 7, in the transmit mode, the LNA is disabled when the switch sw0 is off and sw1 on. Thus, the M/N is used for the output power-matching circuit for the DA. The DA delivers its high output power to the antenna efficiently without any signal loss caused by the T/Rx switch. The simulated power-added efficiency (PAE) of the proposed DA is 36.5%. The input transistors M_G and M_S of the LNA are protected from the DA's large output power with both dc-isolation by sw0 and AC-isolation by sw1. In the T/Rx switch, the p-MOS switch sw0 has a high body voltage of V_{DD2}=2.3V through a high value resistor R_B such that its drain and bulk are protected from break down. In the receive mode, the DA is disabled when sw0 is on and sw1 off. The single-ended input of the LNA is directly dc-coupled to M/N, which is used for LNA's input-matching circuit and dc current path for M_G. Loss caused by sw0 at the LNA input is below 1.1dB in the 900MHz frequency range from simulation results.

The LNA in Fig. 7 adopts a noise cancelling topology [6], which comprises a non-inverting signal path (M_G) and an inverting signal path (M_S) for noise-cancelling and single-ended-to-differential signal conversion. The simulated NF of the proposed LNA with the T/Rx switch is 3.9dB. Its single-ended input is connected to the single-ended output of the DA, and its differential output is connected to the following double-balanced passive mixer. In the LNA, since transconductances of the input transistors M_G and M_S are set to be equal to reduce dc power consumption, the impedance value of two *RLC* loads is also identical. Under this condition, the thermal noise from M_G can be cancelled at the differential output and the fully differential output voltage signal can be achieved. The proposed LNA provides a high voltage gain of 30 dB and a low voltage gain of 10 dB to accommodate an RF input signal in a range from the minimum sensitivity level of -105 dBm to the maximum input level of -20 dBm. It draws 3.3 mA from a 1.8 V supply voltage.

In the proposed zero-IF receiver shown in Fig. 6, since the down-converted IF signal has occupied from 5.208 kHz, flicker noise may be troublesome for the receiver's sensitivity. To solve this problem, an quadrature current-driven passive mixer has been adopted in this work, as shown in Fig. 8, which provides little or no flicker noise while providing a high linearity in the receive path. However, passive mixers have no reverse isolation. As a result, in passive mixers with 50% duty-cycle, an IQ crosstalk problem occurs since one mixer switch

from the I channel and the other mixer switch from the Q channel are simultaneously ON at a given moment [7]. To mitigate this IQ crosstalk problem, 25% duty-cycle passive mixers [7], [8] and an LO-2LO mixer [9] have been previously reported. However, these approaches [7]-[9] tend to require more complex LO-generation circuits and higher DC power consumption

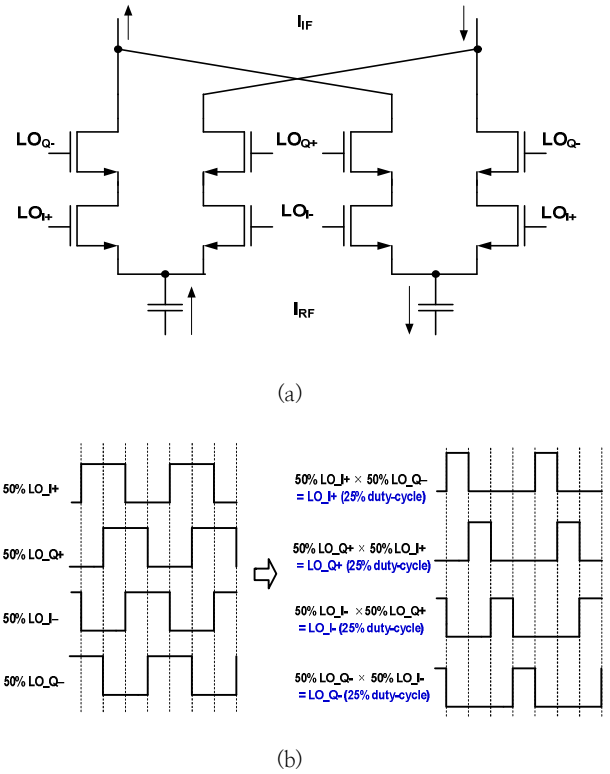

Fig. 8. (a) Proposed current-driven passive mixer (I-path) and (b) effective 25% duty-cycle clock generation using 50% duty-cycle clocks.

than those adopting 50% duty-cycle. Therefore, a quadrature passive mixer topology presented in [10] has been modified and then utilized in this work. Fig. 8-(a) shows the proposed current-driven passive mixer (only I-path), in which two switches are connected in series to form an AND function for two 50% duty-cycle LO clocks to achieve a 25% duty-cycle switching effectively. For example, in Fig. 8-(b), multiplication of two 50% duty-cycle LO clocks, $LO_{\_I+} \times LO_{\_Q-}$, effectively generate a new 25% duty-cycle $LO_{_I+}$clock. In this way, the proposed passive mixer is effectively driven by 25% duty-cycle LO clocks, which can eliminate the IQ crosstalk in the receiver. The current conversion gain of the proposed current-driven passive mixer shown in Fig. 8-(a) can be briefly expressed as

$$\left|\frac{I_{IF}}{I_{RF}}\right| \approx \frac{\sqrt{2}}{\pi}, \tag{1}$$

where I_{RF} and I_{IF} are a differential RF current signal and a differential IF current signal, respectively. This current conversion gain in (1) is equal to that of a 25% duty-cycle current-driven passive mixer [7]. Finally, the proposed current-driven passive mixer can solve the IQ crosstalk problem without degradation of other aspects of performance, requiring no additional circuits or additional DC power consumption.

Fig. 9 shows the proposed analog baseband circuit (only I-path), comprising a channel-selection LPF, four resistive-feedback VGAs, and a dc offset cancellation (DCOC). The proposed analog baseband circuit provides a voltage gain of 70 dB in 1 dB step with a cutoff frequency from 100 kHz to 600 kHz depending on the channel bandwidth in use.

In general, since active RC LPF shows higher linearity than G_m-C LPF, a 5th-order active RC Chebyshev LPF [11], [12] has been adopted in Fig. 9. In Fig. 9, the 1-dB cutoff bandwidth of the channel-selection LPF is given by $1/(R_s C_{1-5})$ and controlled by the digitally-controlled capacitor C_{1-5} for high immunity of process, voltage, and temperature (PVT). In Fig. 9, VGA1 [13], which can provide a voltage gain of 24 dB, is followed by the channel-selection LPF to suppress flicker and thermal noises generated from the following circuits, while other VGAs are located after the channel-selection LPF for considering linearity. In Fig. 9, the channel-selection LPF and four VGAs use the same OP-amp, which is a two-stage configuration [13] with large input devices to suppress flicker noise at low frequency. The designed Op-amp shows a DC gain of 65 dB and a differential-mode phase-margin of 100° at a unit-gain bandwidth of 72 MHz, drawing 395 μA

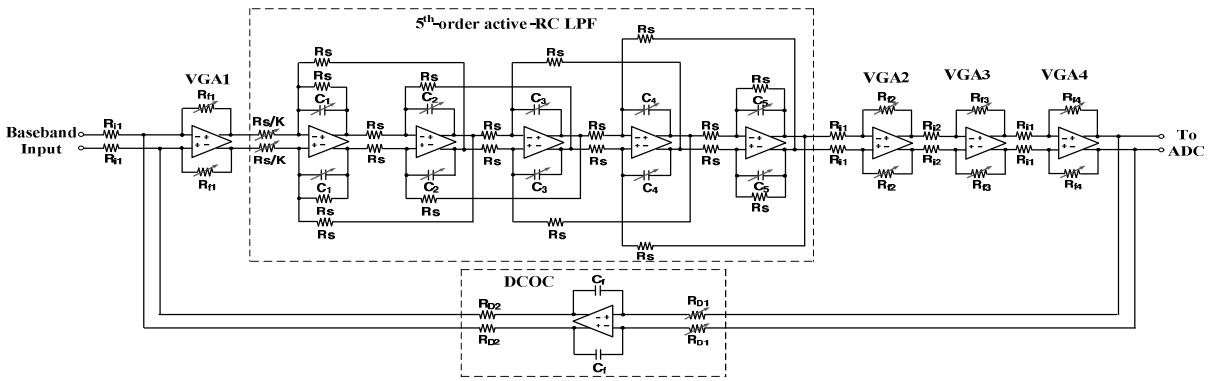

Fig. 9. Proposed baseband circuit (I-path)

from a 1.8 V supply voltage. Measured output spectrum of the receiver has been shown in Fig. 10.dc-offset cancellation in a zero-IF receiver is inevitable since dc-offset may saturate the baseband output. As shown in Fig. 9, to solve the DC-offset problem, a DCOC loop has been built based on voltage-current negative feedback. In Fig. 9, the cutoff frequency of the DCOC is set around 2 kHz since active-subcarriers occupy from 5.208 kHz [3]. However, due to the low cut-off frequency in this work, the required capacitances C_f is 5 mF which cannot be integrated on a chip. Thus, they are externally implemented at the cost of pads. To achieve a constant cutoff frequency in DCOC, the value of input resistor R_{D1} in DCOC digitally decreases as the voltage gain by a LPF and four VGAs in the forward path decreases. The post-layout simulation shows that the analog baseband output can be tolerated up to a 400 mV input DC offset. The OP-amp used in the DCOC consumes about four times the dc current in the 2nd-stage compared to other OP-amps to have a

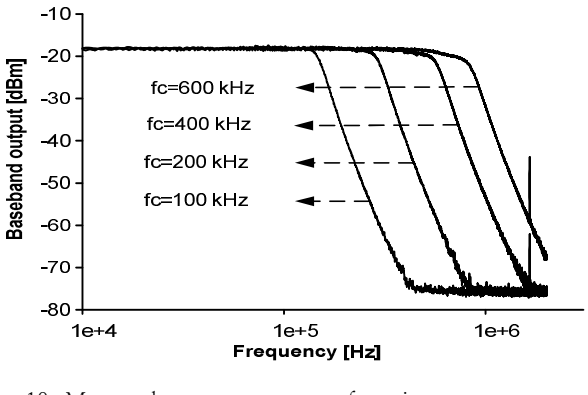

Fig. 10. Measured output spectrum of receiver.

high zero frequency for loop stability and to provide enough feedback current through R_{D2}. The total dc current consumption for IQ analog baseband circuits is 9.8 mA from a 1.8 V supply voltage.

In the proposed IQ direct-conversion transmitter shown in Fig. 6, quadrature analog baseband signals from digital-to-analog converters (DAC) are applied to a highly linear quadrature 5th-order active-RC LPF, and then subsequently to an IQ VGA with a 6 dB gain range. For IQ modulation and frequency up-conversion, a quadrature voltage-mode passive mixer has been utilized in this work since it provides higher linear characteristics, requires no dc power consumption, and has a smaller chip area compared to the Gilbert active mixer. Fig. 11 shows the proposed up-conversion passive mixer, where two switches are also connected in series to form an AND function for two 50% duty-cycle LO clocks to achieve a 25% duty-cycle effectively the same as the down-conversion passive mixer in Fig. 8. Since this configuration mitigates the unwanted IQ crosstalk in the proposed IQ direct-conversion transmitter, the two RF sides of the mixers do not need to be buffered by two transconductors [14], leading to smaller chip area and lower dc power consumption. Though the proposed passive mixer is designed with a single-ended topology to drive the following single-ended DA, it does not produce LOleakage to its single-ended output [14], [15].

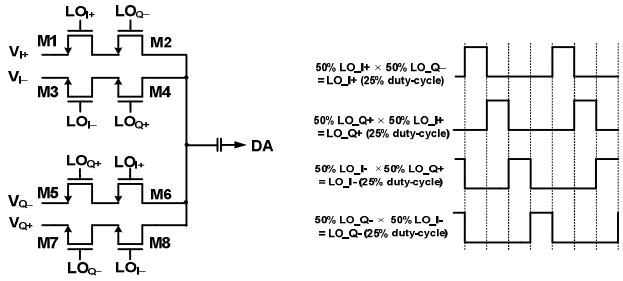

Fig. 11. Proposed up-conversion passive mixer.

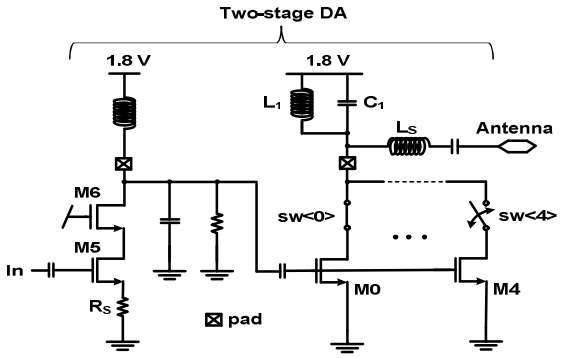

Fig. 12. Simplified two-stage driver amplifier.

In the proposed up-conversion passive mixer, if the IF quradrature-input-voltage signals are $V_{I\pm}$= $\pm$Acosw$_{IF}$t and $V_{Q\pm}$=$\pm$Asinw$_{IF}$t, the up-converted output voltage signal $V_{RF,out}$ can be expressed by

$$V_{RF,out}(t) \approx \frac{2\sqrt{2}}{\pi} A\cos(\omega_{RF}t + \phi), \qquad (2)$$

where A is the amplitude of IF voltage signals, and f is a phase delay. From (2), the voltage conversion gain is -0.9 dB and is equal to that of the 25% duty-cycle single-ended passive mixer described in [15].

Fig. 7 shows the proposed driver amplifier. Considering linearity and power efficiency, the proposed DA has been designed as a single-ended two-stage topology; it comprises class A and classAB amplifiers. As shown in Fig. 7, the first stage amplifier (M_5 and M_6) with an *RLC*

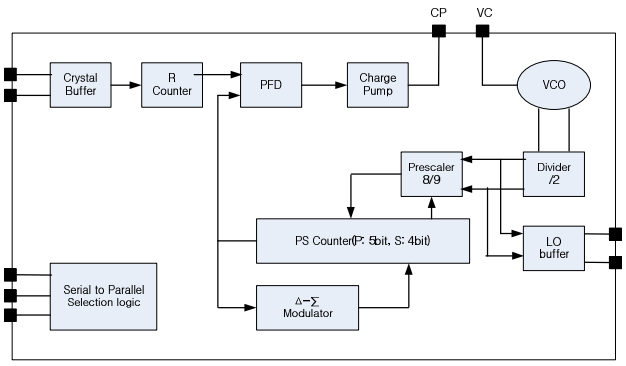

Fig. 13. Block diagram of PLL.

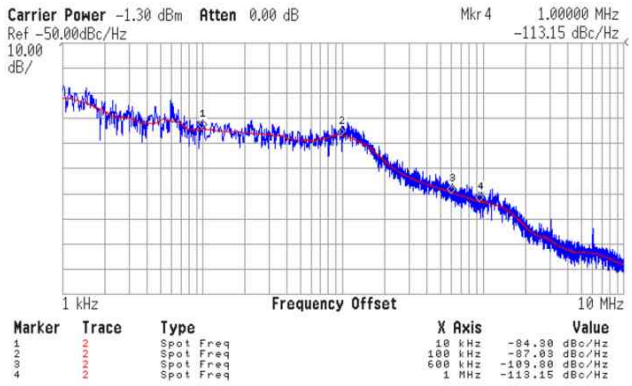

Fig. 14. Measured phase noise.

resonate load is biased in class A mode and also source-degenerated by R_S to achieve high linearity. It provides a high voltage swing for the following class AB amplifier with a moderate gain and high linearity. The second-stage amplifier is a cascode common-source class AB amplifier, where the amplifier transistors are split into binary scaled units (M_0 to M_4) that can be turned on or off by thick-oxide cascode transistor switches of sw〈0〉 to sw〈4〉 such that dc power consumption is proportional to the output power level. In Fig. 12, the variable output power range of the overall DA is from −10 dBm to +10 dBm and the corresponding dc power consumption is from 8.1 mW to 24.3 mW. To achieve a high output compression point with a 1.8 V supply voltage, the output of the second stage is power-matched instead of gain-matching by using a series inductor *Ls* and resonant circuit (L_1 and L_2) at the cost of gain reduction of 1.5 dB. In Fig. 12, all inductors used for DA are externally implemented

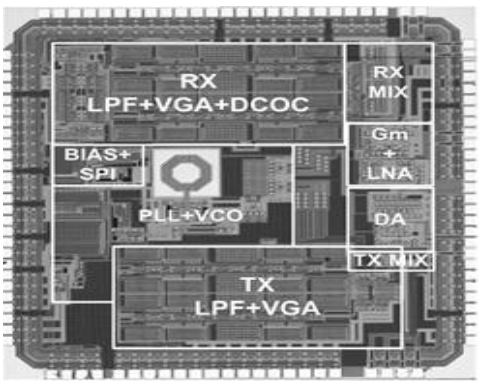

Fig. 15. Photo of the fabricated RF tranceiver chip.

for smaller chip size. Fig. 13 shows a block diagram of the proposed $\Delta\Sigma$ fractional-N frequency synthesizer. It uses a 24 MHz reference clock with a complementary differential VCO running at twice the LO frequency of 1.4-to-2 GHz. A divide-by-two circuit converts the differential VCO output signal to quadrature 920 MHz LO signals for the up-and down-conversion passive mixers shown in Figs. 8 and 11. The 3rd-order three-bit output $\Sigma\Delta$ modulator improves the closed-in phase noise and provides a resolution of 91.55 Hz. The measured output phase noise is shown in Fig. 14, which is −84 dBc/Hz at a 10 kHz offset and −113 dBc/Hz at a 1 MHz offset, respectively.

VI. Measurement Results

As shown in Fig. 15, the proposed RF transceiver has been fabricated in 0.18-μm CMOS technology as a second prototype. The first fabricated RF transceiver has been briefly introduced in [16]. In Fig. 15, the chip area including pads is 2.8-mm × 3.0-mm. The fabricated RF transceiver consumes 37 mA in Tx mode and 38 mA in Rx mode for a 1.8 V supply voltage.

Fig. 16 shows the transmitted output spectrum for option 1, which is QPSK-modulated with a data-rate of 800 kbps. Considering a PAPR of +10 dB in the transmitter, the measured average channel power is −2.7 dBm (including cable losses).

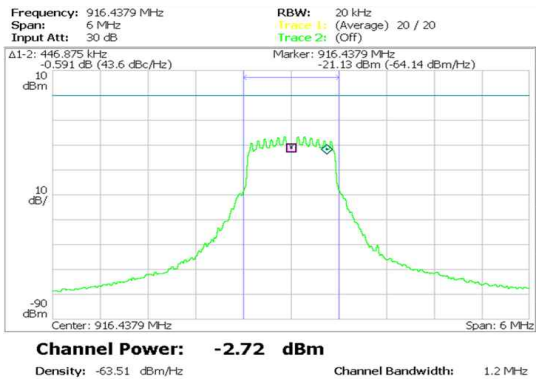

Fig. 16. Transmitted output spectrum for option 1.

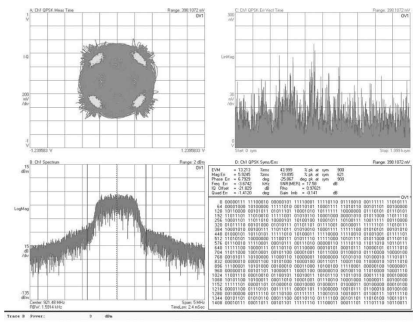

Fig. 17. Measured Tx EVM at +3dBm; QPSK-modulated baseband signals generated from a vector signal generator (VSG) have been applied to the input of the transmitter for the test of Tx EVM.

For testing of Tx EVM, QPSK-modulated quadrature baseband signals, which have been generated from a vector signal generator (VSG), are applied to the transmitter inputs. As shown in Fig. 17, the measured Tx EVM is about 13% (−17.7 dB) at the channel power of +3 dBm, but EVM is −20 dB at the power of −2 dBm. The receiver output baseband spectrum for option 1 is shown in Fig. 17. It has a bandwidth of 600 kHz and a

good stop-band rejection ratio. To measure the receiver sensitivity, a SUN OFDM system board is designed as shown in Fig. 19. It consists of three different PCBs; the upper PCB is for the RF chip,

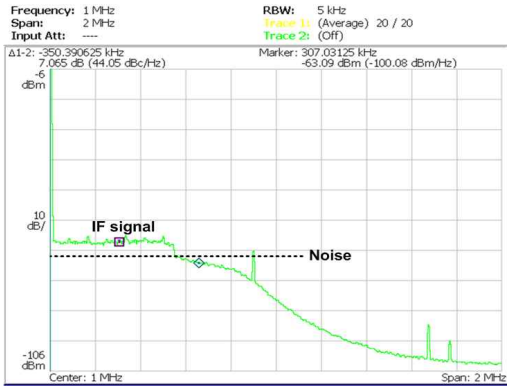

Fig. 18. Baseband output spectrum for option 1 (channel BW=600 KHz).

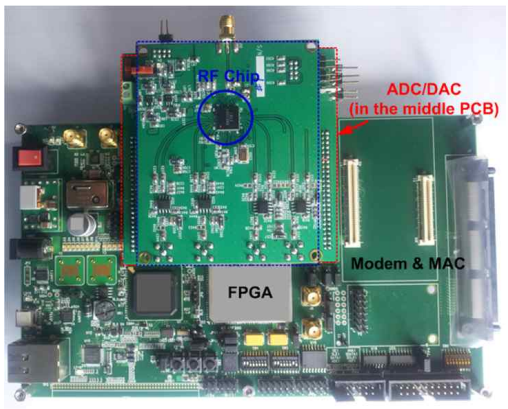

Fig. 19. SUN OFDM system board consisting of RF, Modem, and MAC.

Table IV.
Performance summary for option 1.

	Measured Results	Standard [3]
NF	-	< 10 dB
Sensitivity level		
@ 100 kbps	-103 dBm (PER<1%)	-103 dBm (PER<10%)
@ 200 kbps	-102 dBm (PER<1%)	-100 dBm (PER<10%)
@ 400 kbps	-101 dBm (PER<1%)	-97 dBm (PER<10%)
@ 800 kbps	-98 dBm (PER<1%)	-94 dBm (PER<10%)
Rx Input P_{1dB}	-11 dBm	> -20 dBm
Rx IIP3	-2.3 dBm	
Tx average power	-2 dBm	> -3 dBm
Tx EVM	-17.7 dB @+3dBm*	> -10 dB
Tx output CP_{1dB}	+10 dBm	-
Phase Noise PLL	-113dBc/Hz @1MHz	-
Rx mode current	38 mA	-
Tx mode current	37 mA	-
Supply voltage	1.8 V	-
CMOS Tech.	0.18-μm	-

*For QPSK modulation signals from a vector signal generator (VSG).

the middle PCB for the ADC/DAC, and the bottom layer for the Modem and MAC. ADC and DAC have been implemented in 0.18-μm CMOS technology, and Modem and MAC are designed with FPGA. Using this board, the sensitivity level of the fabricated RF transceiver has been evaluated. The measured minimum sensitivity for a data-rate of 100 kbps is -103 dBm with a PER of 1%. This measured sensitivity level has satisfied with the IEEE 802.15.4g SUN OFDM standards, which is -103 dBm for PER < 10% at 100 kbps. Table IV summarizes the measured RF transceiver performances for option 1.

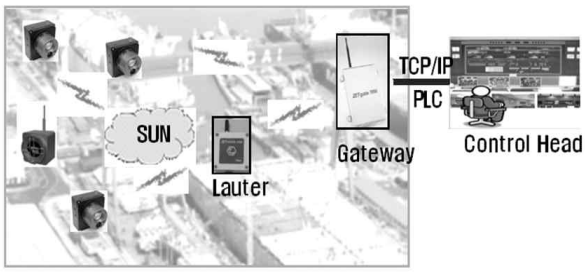

Fig. 20. Conception of public demonstration at ship dockyard.

VII. Public Demonstration

There are numerous potential SUN applications in many wireless connection fields. One target application could be in ship dockyards, as shown in Fig. 20. During welding processes, lives and cost can be saved by distinguishing between a real fire and sparks with our SUN system. In general, because the distance from construction sites to the control head is very long, it is very difficult to distinguish at the latter. The public demonstration shows a feasible solution. When a spark is produced at a welding site, a smart camera takes a picture and sends it to the control head with the help of our SUN wireless system. The control head can then easily judge is there is an actual fire. The concept and public demonstration are shown in Figs. 20 and 21, respectively.

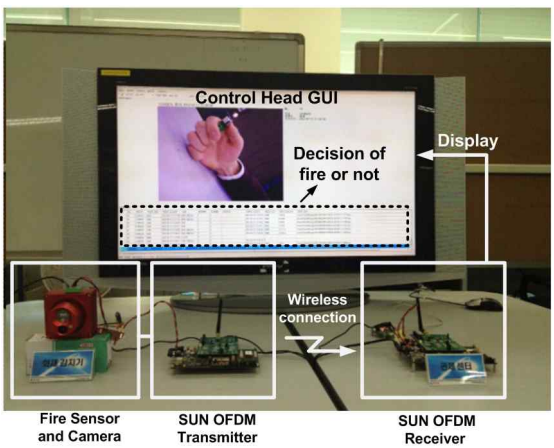

Fig. 21. Public demonstration of ship dockyard.

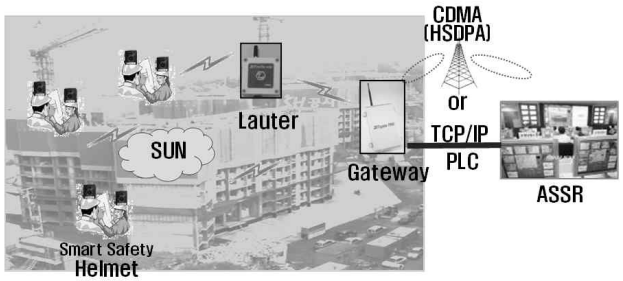

Fig. 22. Conception of public demonstration in construction sites.

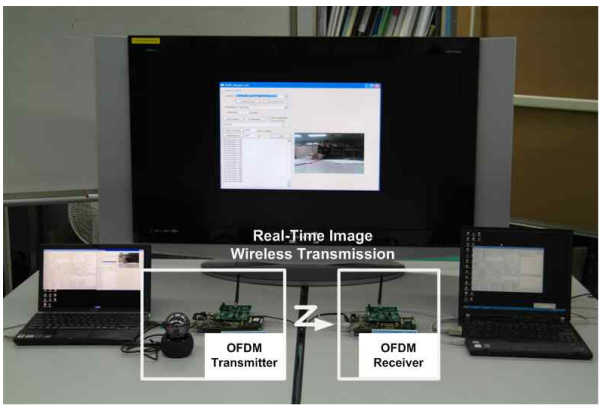

Fig. 23. Public demonstration of construction site application.

Many construction sites also would benefit from our SUN system. In Fig. 22, when an emergent decision is needed at a construction site, captured real-time video images, which can be captured by a smart safety helmet, are sent to the all-source situation room (ASSR) by our SUN system and Gateway. This service will be prearranged starting in 2015. The public demonstration of this service, where real time images were transmitted and received, is shown in Fig. 23.

VIII. Conclusion

This paper has presented a proposed IEEE 802.15.4g SUN OFDM-based RF transceiver, which is implemented in 0.18-μm CMOS technology. Measurement results show the fabricated RF transceiver chip favorably supports the IEEE 802.15.4g SUN OFDM standard. With the implemented SUN OFDM system consisting of the RF, Modem and MAC, two successful public demonstrations have been carried out, which show the high possibility of exploiting SUN wireless links in many commercial fields.

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