Design of a wireless transceiver in 0.18um CMOS technology for LoRa application

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***Abstract* – The design circuit will cover the design and study of CMOS wireless transceiver for Long Range Radio (LoRa) application. As the communication method, it adopts Chirp Spread Spectrum (CSS) modulation which has low power and excellent processing gain and is designed as a transceiver structure suitable for long distance communication. A direct-conversion transceiver that does not use an intermediate frequency is analog to digital converter (ADC), a digital to analog converter (DAC), a low-pass filter (LPF), a variable gain amplifier (VGA), a low noise amplifier (LNA), power amplifier (PA), and Phase Locked Loop (PLL) blocks. This RF chip is designed for the 018um process, with a supply voltage of 1.8V and a maximum operating frequency of 950MHz.**

***Keywords*—LoRa, transceiver, DAC, LNA, PLL, LPF, VGA, pipelined ADC, 018um CMOS process**

I. INTRODUCTION

Recently, the demand for wireless communication of information for Internet of Things (IoT) and Machine to Machine (M2M) Networks has been rapidly accelerated due to popularization of smart phones, and the establishment of a fixed or mobile wireless communication infrastructure is becoming more and more urgent. The Low-Power Wide Area Networks (LPWAN) such as of SIGFOX, UNB, LoRa, or NB-IoT has emerged as the main mechanism for Internet access in campuses, hospitals, airports and other public places. By 2020, it is estimated that more than a billion smart devices will have LPWAN technology. Especially, long-range (LoRa) wide-area networks has long battery life and excellent coverage [1]. Due to extensive application and market potential, the demand of System on chip for LoRa is high.

In this paper, we designed and studied the Chirp Spread Spectrum (CSS) used in the physical layer of the LoRa infrastructure that can achieve higher battery performance by keeping the radio frequency (RF) link budget constant while lowering the transmitter power [2].

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The RF receiver consists of an LNA and a mixer, and the LNA makes a small signal from the antenna large. The LNA acts as a voltage amplifier and minimizes noise. The amplified signal enters the mixer and the signal is down-converted from RF to IF. This IF signal is digitized by the ADC. With an increasing demand to process a large amount of data in communications systems, higher resolution and bandwidth is necessary. Among various structure of ADCs, pipelined ADC has been widely used for high resolution applications. This proposed design is focused on implementation of 10-bit pipelined ADC in 0.18um CMOS technology [3-4].

The PLL frequency synthesizer operates in such a manner that the output frequency (f_{vco}) of the actual VCO is compared with the phase of the reference frequency and fixed to the phase of the reference frequency. First, a voltage is applied to the VCO to generate an output frequency. The output frequency is divided into a frequency divider included in the feedback loop and then compared with the phase of the reference frequency in the phase frequency detector. The Phase frequency detector (PFD) compares the reference frequency with the phase of the output frequency of the frequency divided voltage oscillator. The charge pump (CP) pushes or pulls charges corresponding to the pulse width of each signal in accordance with the Up and Down signals output through the PFD [5-6].

II. ARCHITECTRUE

A. Transceiver block diagram

This research is about wireless transceiver. Fig. 1 shows a structure of transceiver. Transceiver includes DAC, LPF, VGA, Mixer, PA, PLL, LNA and ADC blocks.

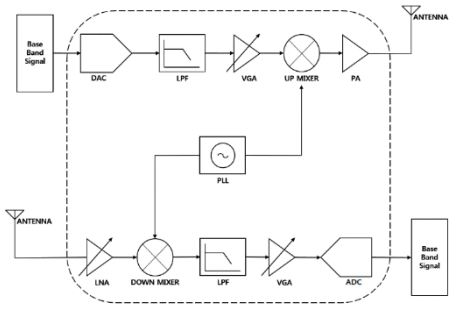


Fig. 1. Block diagram of Transceiver

B. DAC

Generally, it is composed of segmented type. However, if the delay time difference and resolution of the input signal are increased by sub-DAC having different structures, the resolution of the two structures increases as well, which may cause disadvantages in the two structures. Therefore, the 3bit thermometer decoder is implemented in 3 stages considering chip area and performance, and the delay time between the input signals is eliminated by using the latch at the digital input terminal of the DAC in the whole structure [7].

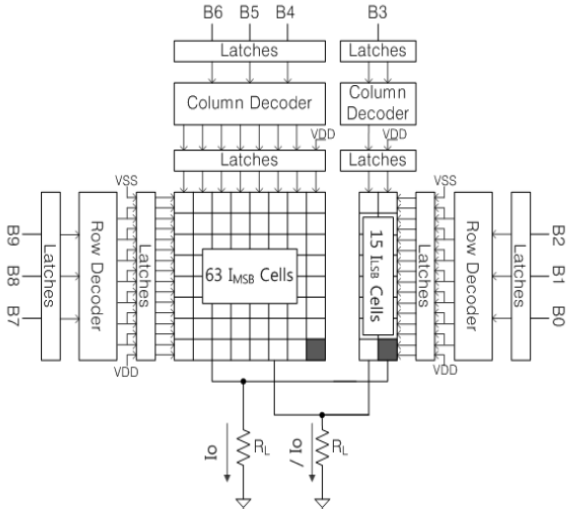


Fig. 2. 10-bit DAC with thermometer decoder

C. LNA

Unlike a typical LNA structure, a circuit for performing an active inductor function using a CMOS transistor was constructed to minimize the effect of the parasitic capacitance at low power consumption, small area charge, and high frequency.

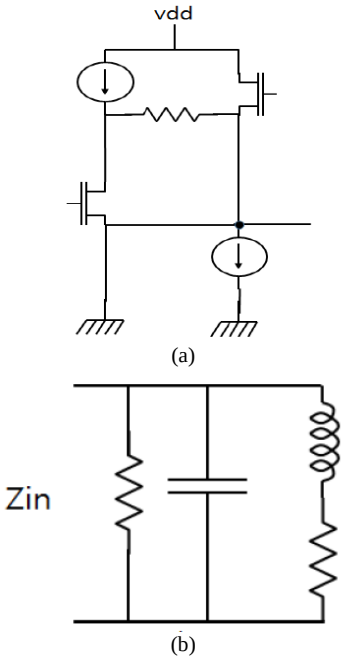


Fig. 3. (a) Active inductor circuit, (b) Active inductor equivalent circuit

D. Pipelined ADC

To obtain high bandwidth and high DC gain with a low supply voltage, it has folded-cascode amplifier with a gain boost technique. Fig. 4 shows the 20MS/s 3-stage pipelined ADC. By using correction circuit for output digital bits, it outputs the 10-bits with overlapping the one bit of each stage. This structure helps low-power and high-speed. Fig. 5 shows the schematic of the amplifier used in the SHA and MDAC. To obtain a high bandwidth and high DC gain, it has folded cascode topology.

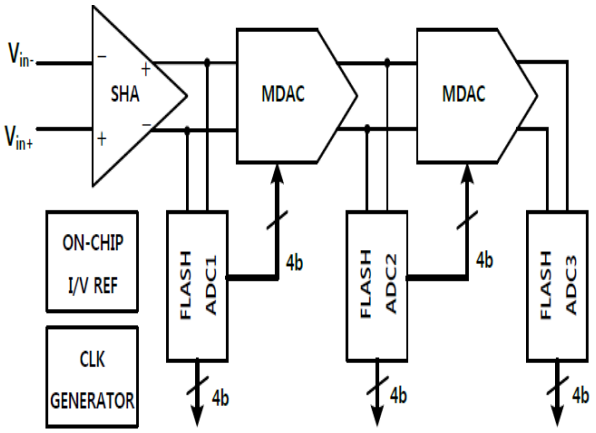


Fig. 4. Block diagram of 10-bit pipelined ADC

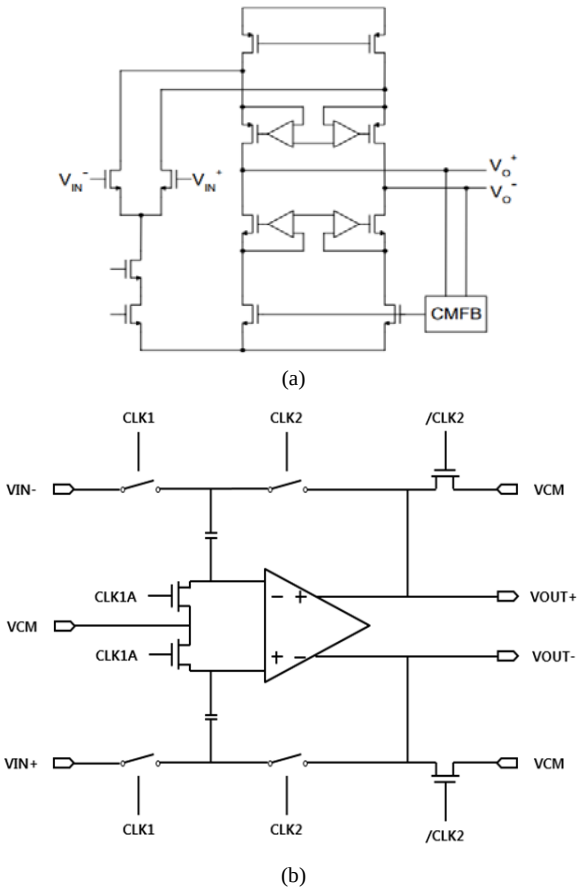


Fig. 5. (a) Circuit Diagram of Folded Cascode Amplifier, (b) Sample and Hold amplifier

E. PLL

PLL of this transceiver is targeting for LoRa band which is suitable for long range communication [8]. It expanded bandwidth and made good noise figure by adding chirp spread spectrum (CSS) modulation structured with binary delta-sigma modulation. Spread spectrum system expands bandwidth of transmission more than one of data signal, it makes processing gain which reduce error rate of communication. CSS has better processing gain than Direct Sequence (DS), Time hopping (TH) and Frequency hopping(FH). Transmitter and receiver have frequency out with 50MHz span in ISM band by using chirp signal. Fig. 6 shows spreading spectrum sequence of CSS.

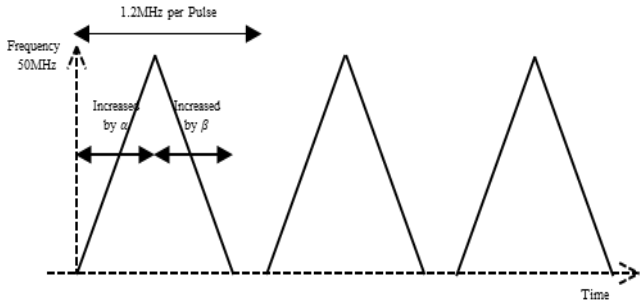


Fig. 6. Sequence of Chirp Signal Generation

VCO of PLL is Quadrature LC tank Oscillator. It has four output each has 90° difference with each other's. It has 1.5V voltage sweep range and 300MHz frequency sweep range. Fig. 7 shows structure of VCO.

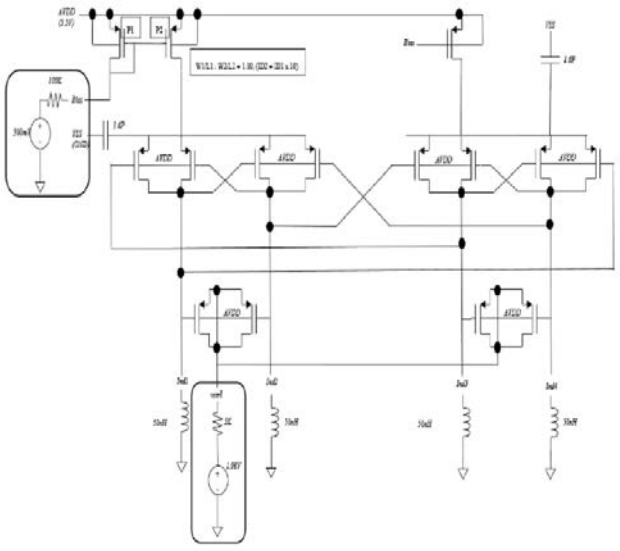
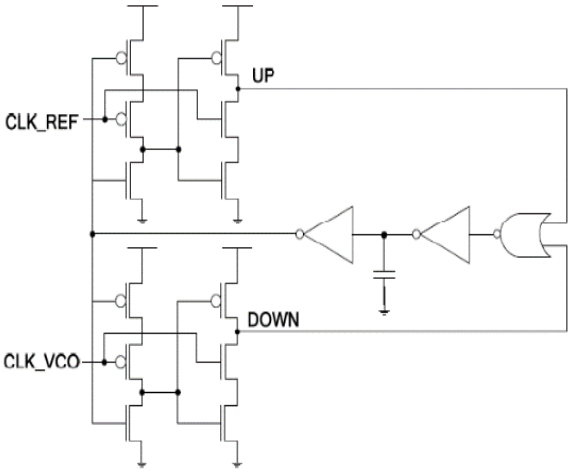
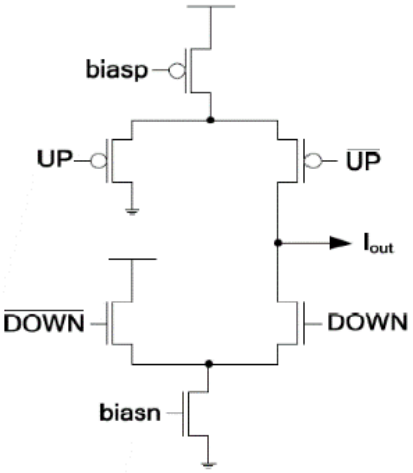


Fig. 7. Structure of Quadrature LC tank Control Voltage Oscillator

Phase Frequency Detector (PFD) is structured with TSPC D-flip flop [9]. Output of PFD is pushing or pulling charge pump (CP), then charge pump makes current for loop filter. Fig. 8 shows structure of PFD and CP.



(a)



(b)

Fig. 8. Structure of (a) PFD, (b) CP

III. RESULTS AND DISCUSSIONS

The proposed LNA to LPF are illustrated in Fig. 3 and the result of simulation are shown in Fig. 9. we can see the simulation results of Mixer to Power Amplifier driver from Fig. 10.

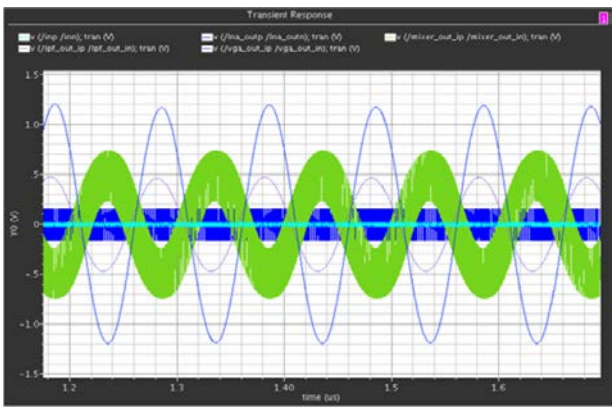


Fig. 9. Transient waveform of LNA to LPF

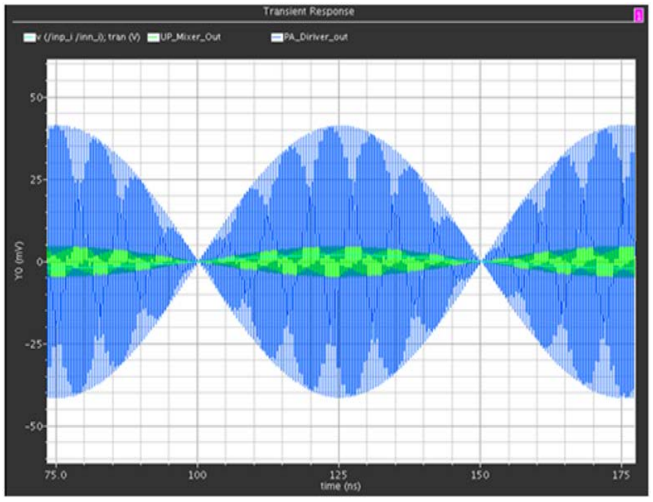
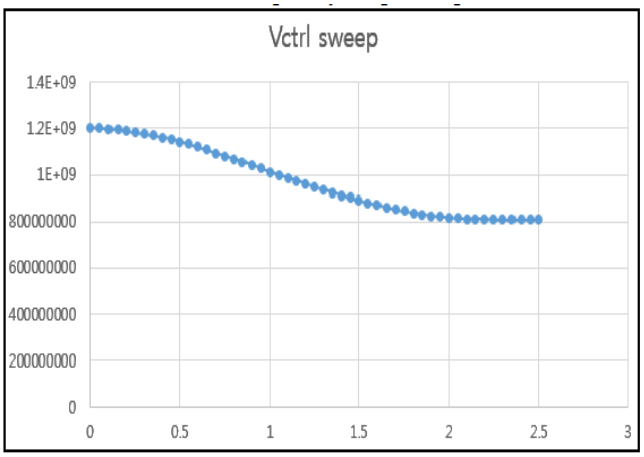
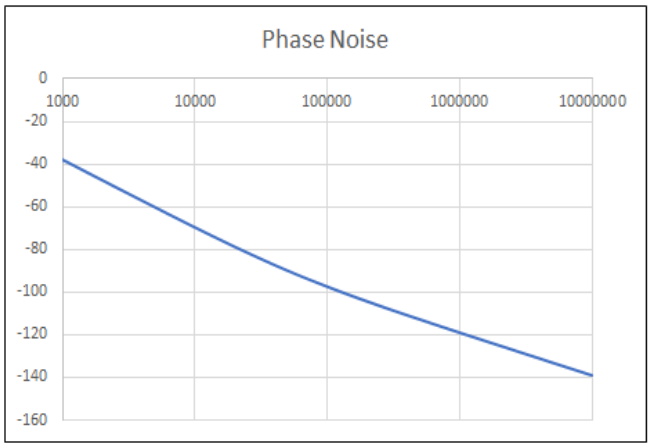


Fig. 10. Transient Waveform of UP Mixer to Power Amplifier Driver

The Fig. 11 shows sweep range of VCO and phase noise VCOs. Table I shows performance summary of the proposed VCO. The Figure 12 shows control voltage. It took 72us for PLL to be locked. As the simulation of CSS is controlled by SPI, the simulation results in Fig. 13 show that transceiver have frequency out with 50MHz span in ISM band by using chirp signal.



(a)



(b)

Fig. 11. (a) Frequency & Voltage Sweep Range of VCO, (b) Phase Noise of VCO

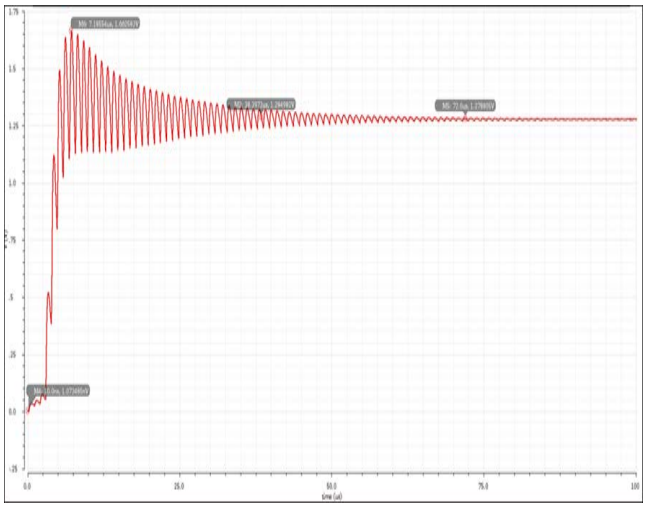


Fig. 12. Locking test of PLL

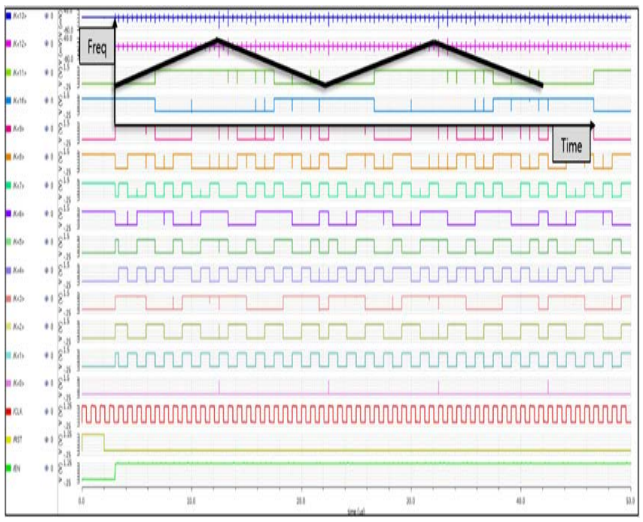


Fig. 13. Transient Waveform of Chirp Signal Generator

The performance summaries of VCO and pipelined ADC are shown in TABLE I and II. As shown in Table III, this RF Front End system has better performance relative to [10], [11]. This comparison of these parameter is summarized in Table III.

TABLE I.
Performance summary of VCO

Parameter	Result
Process	0.18 μm CMOS
DC power	1.8 V
Frequency output	800 ~1150 MHz
Control Voltage Range	0.3 ~ 1.5V
Phase Noise	-97.956dBc/Hz @ 100KHz
Power Consumption	25mW

TABLE II.
Performance summary of pipelined ADC

Parameter	Result
DC power / Current	1.8 V/16 mA
Resolution	10 bits
Sampling Clock	20 MHz
Input Dynamic Range	1 Vpp
SFDR	48.937dB
Active Die Area	0.662 mm^2

TABLE III.
Comparison with Other Designs for Receiver Front End

	This Work	[10]	[11]
CMOS Technology	180nm	-	65nm
Frequency	850 MHz - 950 MHz	860MHz - 1020MHz	500MHz - 2.5GHz
Supply voltage	1.8V	3.3V	-
Gain	49.8dB	-	38-43dB
Power Consumption	30mW	30mW	12mW

IV. CONCLUSION

In this study, we developed a wireless communication transceiver in the LoRa band using 0.18um CMOS process. LNA and LPF reduce noise during transmission and reception, and control transmit and receive power through programmable VGA. We have reduced the error rate with a PLL with 50MHz span using CSS. In addition, the proposed pipelined ADC improves performance with high resolution and bandwidth. As a result, a low-power and low-error wireless transceiver suitable for long distance communication has been developed.

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