Digital Foreground Self-Calibration of Capacitor Mismatch for SAR ADCs

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***Abstract* - This paper presents foreground digital self-calibration technique for successive approximation resistor (SAR) analog to digital converters (ADCs) is proposed and verified with simulations. Recent advanced in complementary metal oxide semi-conductor (CMOS) technologies and an asynchronous switching allows SAR ADCs to be utilized in a variety of applications. In SAR ADCs, the ADC linearity is mainly limited by capacitor random variation which heavily depends on integrated circuits(IC) processes. The proposed calibration technique effectively averaged out capacitor mismatch errors by taking advantages of anti-symmetric property of mismatch errors in SAR ADCs. This calibration technique significantly reduces capacitor mismatch errors without resorting extensive computation or dedicated circuits. A 12-bit 50 MS/s ADC fabricated in a 65nm CMOS process occupies a die area of 0.12 mm^2. After calibration, a signal-to-noise distortion ratio (SNDR) and spurious-free dynamic range (SFDR) are improved from 44.12 dB to 72.85 dB and 50.59dB to 96.47dB, respectively.**

I. INTRODUCTION

Recent advances in CMOS technologies and an asynchronous switching allow successive approximation register (SAR) analog-to-digital converters (ADCs) to be utilized in a variety of (wideband) applications. In SAR ADCs, the ADC linearity is mainly limited by capacitor mismatch which heavily depends on IC processes. Numerous digital calibration techniques [1-16] have been developed to recover the ADCs linearity beyond the process limit. Those techniques are classified into based on how to errors are corrected. The most common approach is measuring the value of the capacitor weight which is represented by set of digital coefficients. In [1], the weights are obtained by using least-mean-square (LMS) algorithm that minimizes the difference between the two ADC output conversion results. After calibration nonlinearities adaptively equalize to accurate reference ADC. In [2], a small capacitor is used in capacitive digital to analog converter (CDAC) to insert an analog offset signal in signal path. Since same input sampled twice by as single ADC with different sign of the offset, difference can be translated into chance to correct the capacitor weights error. The error can be minimized by LMS algorithm. In [3], use the capacitor in CDAC to introduce a dithering signal and obtain the weight by correlating the output with the pseudo-random dithering sequence. Even though those techniques are effective method to remove capacitor mismatch, it comes at the cost of degraded conversion speed [2], dynamic range [3], and additional reference ADC [1].

In this letter, a digital calibration technique which improves capacitor mismatch with little modification from a conventional SAR ADC is proposed and verified with simulations. Due to property of SAR ADC which will be explained next section, it is possible to improve accuracy of estimated weights by utilizing only averaging. For this reason, the computation complexity associated with post processing is lower than previous techniques using LMS and long pseudo-random sequence. Also it is able to significantly reduce digital circuitry overhead and speed of convergence.

II. PROPOSED DIGITAL CALIBRATION TECHNIQUE

A. Principle of proposed digital calibration

Fig. 1 shows an N-bit conventional SAR ADC employing a binary-weighted SCDAC and an output waveform of the SCDAC. The SCDAC output (V_{SCDAC}) increases or decreases by a certain voltage, which is called a weight, depending on the comparator's decision, as conversion proceeds. Denote W_k as the weight associated with the SCDAC capacitor C_k. The ADC input can be easily reconstructed by using W_k as follows

$$V_{IN}(n) = \frac{V_{REF}}{2} + \frac{1}{2}\sum_{i=0}^{N-1}\left[(-1)^{D_i+1}\cdot W_{N-1-i}\right] + V_Q \quad (1)$$

where D_i ($D_i \sqsubseteq \{0, 1\}$) is the i-th bit value of the ADC output and VQ is the ADC quantization noise. Even though W_k is supposed to be equal to $V_{REF}/2^{N-k}$ for a binary-weighted capacitor array, the actual W_k is deviated

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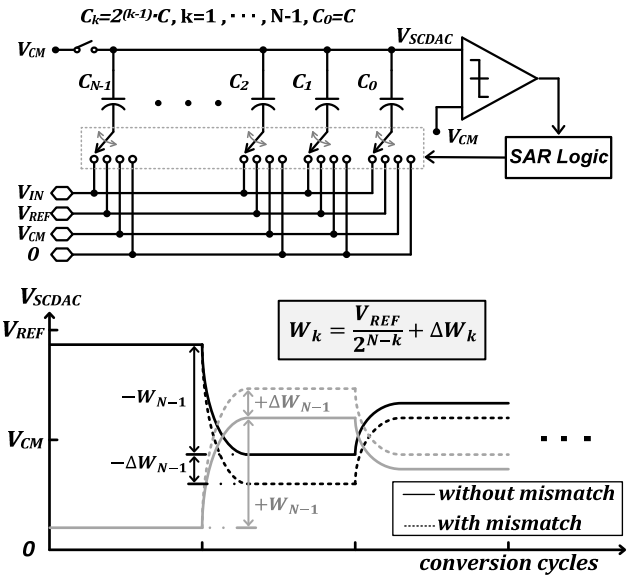

Fig. 1. Conventional SAR ADC architecture and the internal SCDAC output waveform.

from the desired value due to capacitor mismatch. For a given capacitor mismatch between C_k and the rest of the DAC capacitor (ΔC_k), the mismatch induced error on W_k can be either one of the two small voltages having equal amplitude but opposite polarity, i.e., $+\Delta W_k$ and $-\Delta W_k$. Thus W_k becomes $\pm(V_{REF}/2^{N-k} + \Delta W_k)$ and (1) can be rewritten as

$$V_{IN}(n) = \frac{V_{REF}}{2} + \frac{1}{2}\sum_{i=0}^{N-1}\left[(-1)^{D_i+1}\cdot\left(\frac{V_{REF}}{2^{i+1}} + \Delta W_{N-1-i}\right)\right] + V_Q$$
$$= \underbrace{\frac{V_{REF}}{2} + \frac{1}{2}\sum_{i=0}^{N-1}\left[(-1)^{D_i+1}\cdot\frac{V_{REF}}{2^{i+1}}\right]}_{V_{DAC}(n)} + \underbrace{\frac{1}{2}\sum_{i=0}^{N-1}\left[(-1)^{D_i+1}\cdot\Delta W_{N-1-i}\right]}_{V_E(n)} + V_Q \quad (2)$$

where $V_{DAC}(n)$ is an analog representation of the ADC output '$D_0D_1\ldots D_{N-1}$' using the desired weights and $V_E(n)$ is the sum of all weight errors.

The calibration technique is derived from the observation that once ΔW_k is fixed for a given ΔC_k, V_E is solely determined by a digital code and is always antisymmetric around $V_{REF}/2$ because the ADC output is also antisymmetric around mid-code. As a result, an average of V_E approaches zero as the ADC input is swept from 0 to V_{REF}.

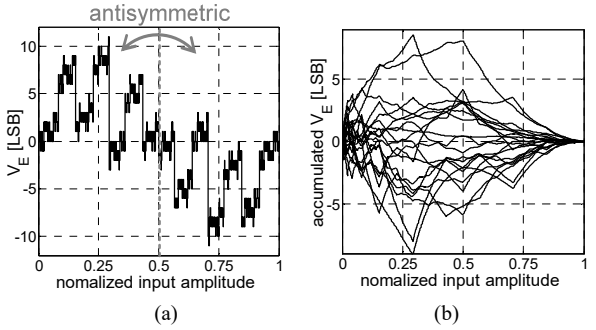

Fig. 2. Capacitor mismatch error simulations for a 12-bit SAR ADC.
(a) VE versus input amplitude
(b) Accumulated VE for 20 different random capacitor mismatches

Simulation results for a 12-bit SAR ADC with 10% random capacitor mismatch are shown in Fig. 2. As can be seen in Fig. 2a, the waveform of V_E is antisymmetric and the accumulated value of VE in Fig. 2b approaches zero as the input amplitude increases to V_{REF}.

B. Capacitor weight estimation method

Fig. 3 shows the operation of proposed capacitor weight estimation method where input analog signal is sampled two different ways. Although the input analog signal path is fully differential for simplicity only positive side representation are shown. When we want to know about k-th capacitor weight, in the step A (refer to Fig. 3. (a)), the input signal V_{IN} is sampled on bottom-plates of all capacitors. Whereas selected capacitor C_k is connected to negative reference voltage "0". Simultaneously, the top-plates voltage is sampled to V_{CM} which is designed to be common-mode voltage $0.5V_{REF}$. Since this scheme follows the V_{CM}-based switching method, before starting conversion, all capacitor bottom plates are switched from V_{IN} to V_{CM}. The top plates are floating and settle to $V_{SCDAC}(n)$

$$V_{SCDAC}(n) = V_{REF} - \left(\frac{C_T - C_k}{C_T}\right)\cdot V_{IN}(n) \quad (3)$$

where C_T is the total capacitance of the CDAC. The ADC converts $V_{SCDAC}(n)$ into a N-bit digital code just like a conventional SAR ADC. The analog representation of the digital code, $V_{DAC}(n)$, can be written as follows

$$V_{DAC}(n) = V_{REF} - \left(\frac{C_T - C_k}{C_T}\right)\cdot V_{IN}(n) + V_E(n) + V_Q(n) \quad (4)$$

In ideal case of SAR ADC, the $V_E(n)$ is zero and $V_Q(n)$ represents quantization error less than ±LSB/2 for a conventional SAR ADC. However, due to capacitor mismatch total error term in (4) no longer less than ±LSB/2 and limit the accuracy of calibration. But it can be defined by ideal quantization error and input correlated raw digital output with capacitor mismatched error components.

$$V_e = (-1)^{B_0}\cdot\Delta W_0 + (-1)^{B_1}\cdot\Delta W_1 + \ldots + (-1)^{B_{N-1}}\cdot\Delta W_{N-1} \quad (5)$$

The next step toward calibrating capacitor nonlinearities is that subtract the V_{IN} information from the step A. During the step B (refer to Fig. 3. (b)). In the sample phase, the top-plates are connected to V_{CM} and bottom-plates of the selected capacitor C_k is connected to positive reference V_{REF}, while all other bottom-plates of capacitor are connected to V_{IN}. After sample, all capacitor bottom-plates are reset to V_{CM}. The top plate are settle to $V_{SCDAC}(n+1)$ as follow

$$V_{SCDAC}(n+1) = V_{REF} - \left(\frac{C_T - C_k}{C_T}\right)\cdot V_{IN}(n+1) - \underbrace{\frac{C_k}{C_T}\cdot V_{REF}}_{W_k} \quad (6)$$

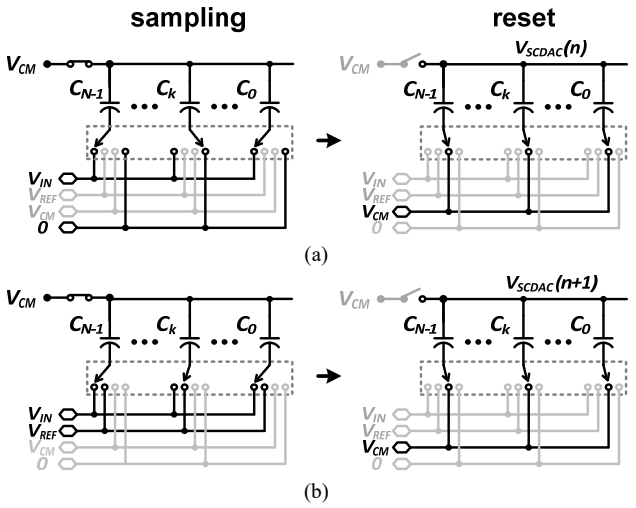

Fig. 3. Proposed DAC switching for estimating weights.
(a) Input sampling with Ck being connected to 0
(b) Input sampling with Ck being connected to VREF

The third term on right hand side of (6) represents k-th capacitor weight (W_k) which is charged by positive reference. The ADC converters $V_{SCDAC}(n+1)$ into a digital code and $V_{DAC}(n+1)$ becomes as follows

$$V_{DAC}(n+1) = V_{REF} - \left(\frac{C_T - C_k}{C_T}\right) \cdot V_{IN}(n+1) - W_k + V_E(n+1) + V_Q(n+1) \tag{7}$$

W_k can be estimated by subtracting (4) from (7) and taking average of the subtracted value over number of M samples.

$$\frac{1}{M}\sum_{n=1}^{M}\left[V_{DAC}(n) - V_{DAC}(n+1)\right] = -\underbrace{\left(\frac{C_T - C_k}{C_T}\right) \cdot \frac{1}{M}\sum_{n=1}^{M}\left[V_{IN}(n) - V_{IN}(n+1)\right]}_{\approx 0}$$
$$\underbrace{-\frac{1}{M}\sum_{n=1}^{M}\left[V_E(n) - V_E(n+1)\right]}_{\approx 0} - \underbrace{\frac{1}{M}\sum_{n=1}^{M}\left[V_Q(n) - V_Q(n+1)\right]}_{\approx 0} + \frac{1}{M}\sum_{n=1}^{M} W_k \approx W_k \tag{8}$$

In the right hand side of (8), the average value of $V_{IN}(n)$-$V_{IN}(n+1)$ is almost negligible because the ramp speed is set to be slow so that the input sample-to-sample variation is kept well below one LSB (i.e., 0.01·LSB). The average values of $V_E(n)$-$V_E(n+1)$ and $V_Q(n)$-$V_Q(n+1)$ are also negligibly small due to the aforementioned antisymmetric property of capacitor mismatch errors and random nature of quantization process, respectively. This process is repeated until all the weights are calculated. For the sake of simplicity, a binary-weighted capacitor array has been adapted in the above analysis, but simulations have been performed with a non-binary capacitor array to avoid a missing decision level as in [4]. The principle procedure of calibration algorithm is shown in Fig. 4.

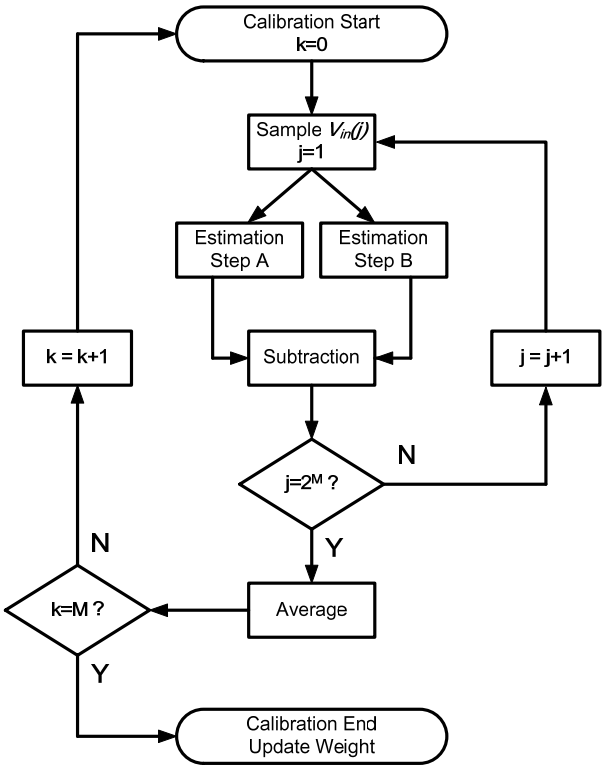

Fig. 4. Flow chart of proposed digital calibration algorithm.

III. PREREQUISITE CONDITION OF PROPOSED DIGITAL CORRECTION

A. Calibration with sinusoidal signal

Calibrating the ADC with a sinusoidal signal is much more cost- effective and convenient, since a slow ramp signal is often generated with a current source and a big capacitor, which take up considerable amount of die area. Also, it is difficult to implement a ramp signal with high linearity. Another difficulty associated with using a ramp is that it is difficult to quantify its distortion levels. On the other hand, sinusoid input can be generated with very low distortion and distortion level can easily be quantified by taking the FFT of the waveform.

However, the calibration technique works with a sinusoidal signal at the cost of slightly increased computational complexity. The calibration process is the same as the one using a ramp signal except that (8) is performed recursively using the estimated Wk. Simulation results reveal that VE is not perfectly antisymmetric and cannott be removed entirely by averaging $V_{DAC}(n)$-$V_{DAC}(n+1)$ with a sinusoidal signal. However, it can be significantly reduced by performing two additional steps. First, $V_{DAC}(n)$ and $V_{DAC}(n+1)$ are recalculated by using the estimated W_k from Equation (8), and then their sample-to-sample differences are averaged again over number of M samples to update W_k. Accuracy of the ADC outputs reconstructed by using the updated W_k is almost the same as the ones calibrated with a ramp signal.

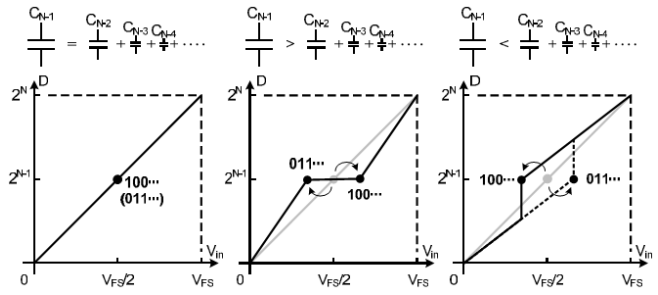

Fig. 5. Transfer curves with radix-2.
(a), super-radix-2 (b), sub-radix-2,(c) in MSB

B. Calibration redundancy

Instead of a conventional binary weighted CDAC scheme, this SAR ADC adopts redundancy to have tolerance to both dynamic and static sources during the conversion. Binary search process has no error tolerance capability for conversion because every analog input has own corresponding digital output code like as one-to-one mapping function. However, sub-radix 2 scheme has redundancy that provides room for making CDAC settling error such that these errors can be corrected in the later conversion steps.

To make the illustration easy, let us assume only the MSB capacitor (C_N-1) suffers mismatch error, while other capacitor are ideal. This boils down to two scenarios. In the first scenario, MSB capacitor is greater than the nominal, which is referred to as super-radix-2. In this case, MSB capacitor is greater than the sum of the rest of the capacitor in the CDAC, which causes a transfer curve shown in Fig. 5 (b). In the horizontal misalignment, there are multiple decision levels mapped to a single digital code. As the analog information is lost and digital correction does not crated decision levels, fatal (digitally uncorrectable) analog to digital conversion errors occur. In contrast, in sub-radix-2 case, MSB capacitor is less than its nominal value. As MSB capacitor is less than the sum of other capacitors in the CDAC, it results in missing codes instead. As shown in Fig. 5 (c), one analog input could be mapped onto multiple digital codes while some of the digital codes would never show up at the ADC outputs in normal cases. However, the error is digitally correctable, because the analog information is preserved.

Maximum radix and minimum number of conversion step are determined by standard deviation of given process productor. Knowing intuitively, large capacitor mismatch requires large redundancy to tolerate, resulting in small radixes and more conversion steps. Taking a 12-bit SAR ADC for example, the relationship between standard deviation, number of conversion step (M), and maximum radix is summarized in table. I.

TABLE I.
Relationship between σ, α, and M

Variation (σ)	Radix (α)	M (ENOB= 11)	M (ENOB =12)	M (ENOB =13)
20 %	1.59	17	18	19
15 %	1.66	15	17	18
10 %	1.75	14	15	16
5 %	1.86	13	14	15
0 %	2	11	12	13

IV. RESULTS

Cadence simulations of a 12-bit SAR ADC employing a non-binary SCDAC with a radix-1.86 were performed to demonstrate the effectiveness of the calibration technique. With 10% capacitor mismatch, approximately 400,000 digital codes were collected to estimate Wk. Table. 2 show the estimation of capacitor weight using the proposed calibration algorithm. Fig.6. shows the dynamic performance of the ADC before and after calibration. The spurious-free dynamic range (SFDR) goes from 50.59 dB to 96.47 dB, the signal to noise distortion ratio (SNDR) is improved form 44.12 dB to 72.85 dB in ramp input condition. Fig.7. shows the dynamic performance of the ADC before and after calibration in case of sinusoidal input condition. Fig.8. shows the simulated SFDR and SNDR learning curves depend on input range.

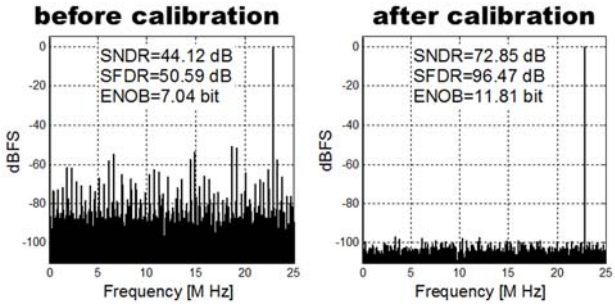

Fig. 6. SAR ADC output spectrums before and after calibration

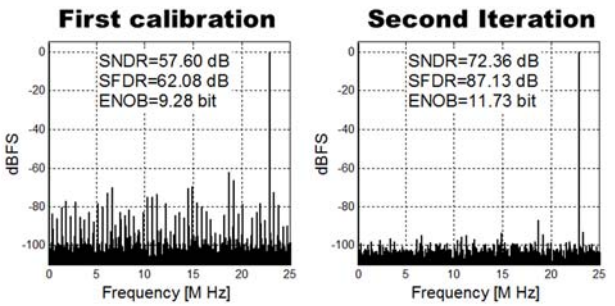

Fig. 7. SAR ADC output spectrums before and after calibration with sine input

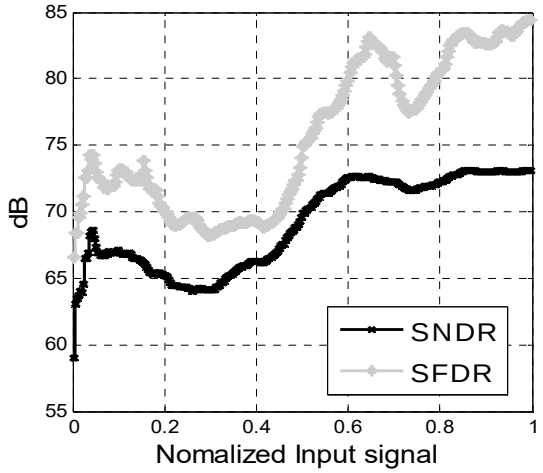

Fig. 8. Simulated SFDR and SNDR learning curves

V. CONCLUSIONS

A foreground digital self-calibration technique has been described. The calibration technique improves capacitor matching without using additional circuit and extensive computation. The circuitry overhead of the calibration is reasonably small compared to previous works, thus proving its practicality. Applied to a 12-bit SAR ADC with 10% capacitor mismatch, SNDR is increased from 44.12 dB to 72.85 dB, resulting in 4.77-bit improvement of ENOB. Improved the ADC linearity and area efficiency will bring the current state-of-the art ADC design with comparable performance by an order of magnitude.

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