A Fully-Integrated High-Voltage Generation IC for Implantable Medical Devices

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***Abstract* - This work presents the design of a fully-integrated high-voltage charge pump IC for implantable medical devices using 0.18-µm CMOS process. The implemented charge pump IC is used to generate high-voltage DC supply of around 12.8 V for the neural stimulator circuit using 3.2-V input voltage with on-chip pumping and load capacitors. The proposed hybrid charge pump IC is comprised of a feed-forward high-efficiency capacitive pumping path and an input voltage modulated feedback regulation path to maintain the output voltage with varying load current of up to 300 µA. The proposed IC achieves around 46% power efficiency at maximum current load condition.**

***Keywords*—Charge pump, High-voltage, Implant device, Neural stimulation**

I. INTRODUCTION

Bidirectional implantable neural stimulation and recording can be used for medical treatment for neural disorders, such as deafness, blindness, and motion disorders [1]-[4]. By recording and analyzing neural signals before and/or after the stimulation, customized stimulation parameters can be decided for each individual and/or better understanding of the stimulation effects can be studied. To enable it, both neural recording and stimulation circuits have to be installed in each electrode and integrated in a single IC with minimized area to achieve small form factor for the overall medical implant device. Considering multi-array systems, the need for small area and low power become an important parameter that need to be addressed in the design process. The basic idea of stimulation is to deliver and recover controlled amount of charge to the tissue through the electrode. However, due to the high impedance of the electrode and tissue interface, high voltage compliance is needed to deliver sufficient amount of charge. On the other hand, low voltage supply is preferred for the neural recording circuits to avoid excessive power consumption. As several supply voltages are required within the IC, a fully-integrated high-voltage generation charge pump (HVGCP) circuit is included to generate the DC supply voltage for the stimulator circuits inside the IC so that the number of pins can be reduced. The HVGCP should be designed with high efficiency considering the limitation of wirelessly transmitted power to the implant from the external device. In addition, the HVGCP should be fully-integrated so that external on-board capacitors do not need to be used which increases the cost and the overall form factor of the implant device. In addition to designing an efficient feedforward charge pump, a regulation function is required to make sure the output voltage does not change with varying load current. Among several schemes, most widely used method is pulse frequency modulation (PFM) [5], [6] which controls the pumping clock frequency depending on the load condition. Although this method has been proven to work well, the efficiency can be degraded due to switching loss at high pumping frequency at heavy load current. This method also has limitation in the load regulation performance at minimal load current.

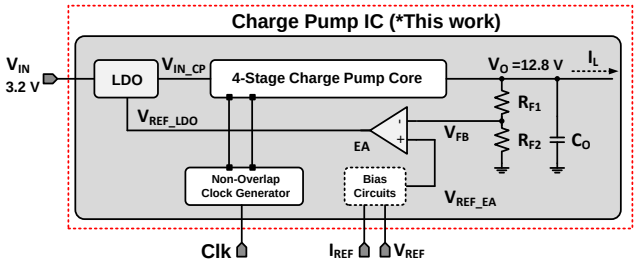

Fig. 1. Block diagram of HVGCP IC

This work proposes a fully-integrated highly-efficient HVGCP employing a hybrid Dickson and Cockcroft-Walton four-stage charge pump core with an input voltage modulated [7] regulation loop to generate a reliable high voltage supply for the neural stimulator. The rest of this paper is organized as follows. The system architecture is presented in Section II. Section III describes the circuit design in detail and Section IV presents the experimental results. The conclusions are given in Section V.

II. ARCHITECTURE

Figure 1 shows the system architecture of the proposed system. This work includes the HV generation charge pump, regulation circuits, non-overlap clock generator, and peripheral bias circuits. The following neural stimulation

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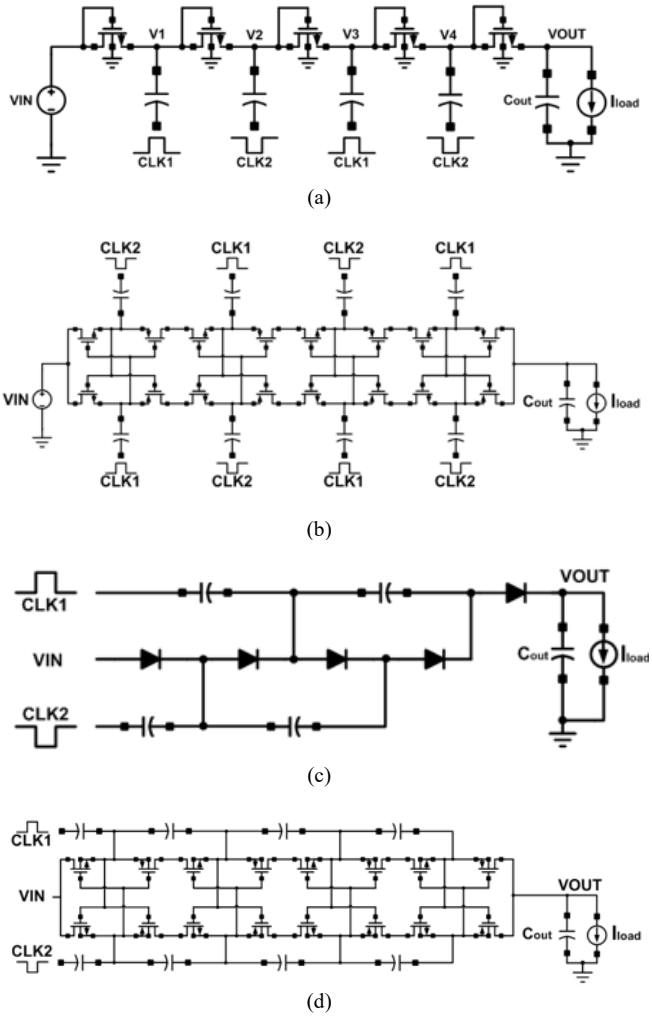


Fig. 2. Conventional charge pump architectures (feedforward path) (a) Dickson charge pump (b) Symmetric Dickson charge pump (c) Cockcroft-Walton charge pump (d) Symmetric Cockcroft-Walton charge pump

circuit, which will utilize the charge pump output voltage as its supply voltage, is assumed to have stimulation current ranges between a few tens of microamperes to maximum current of 300 microamperes. The target output voltage of the charge pump is set to be 12.8 V [8].

A 3.2-V DC voltage is first inputted to the low dropout (LDO) regulator input and after some voltage drop, the LDO output voltage is pumped to 12.8 V output by the four-stage charge pump core. A four-stage hybrid charge pump core circuit based on Dickson and Cockcroft-Walton architectures is proposed for the feedforward path to generate the high-voltage output with good power efficiency using a fixed 40 MHz pumping clock. For the regulation function, a feedback path consisting of resistors R_{F1} and R_{F2}, error amplifier EA, and the LDO block are used to monitor and maintain the output voltage with varying output current load. The charge pump output voltage is fed-back through the resistive divider to the error amplifier and the output of this error amplifier is applied as the reference voltage of the LDO regulator circuit to control the charge pump core input voltage V_{IN_CP} depending on the load current. More details regarding the circuit design is discussed in the next subsection.

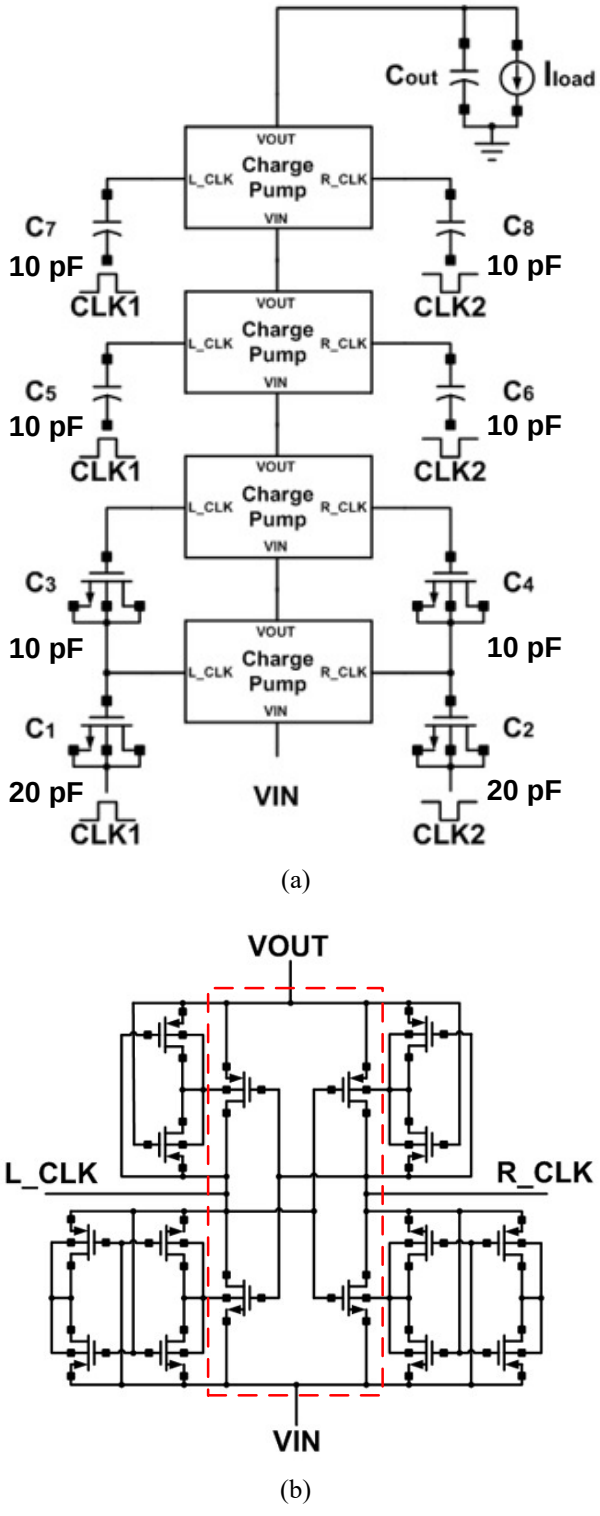


Fig. 3. (a) Proposed architecture of hybrid four-stage charge pump with two-stage Dickson and two-stage Cockcroft-Walton topologies (b) Circuit schematic of symmetrical latched core pumping circuit

III. CIRCUIT DESIGN

Figure 2 shows the previous well-established charge pump topologies that have been proposed. The Dickson architecture [9] in Fig. 2(a) and (b) is well-known for its

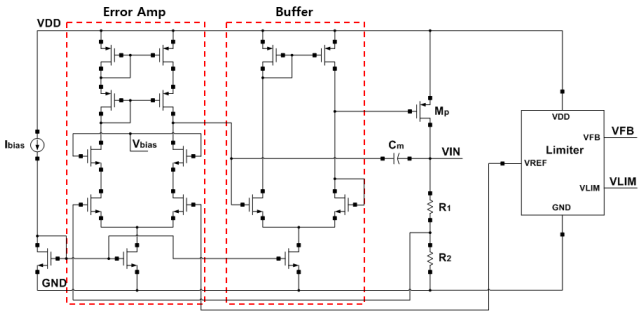
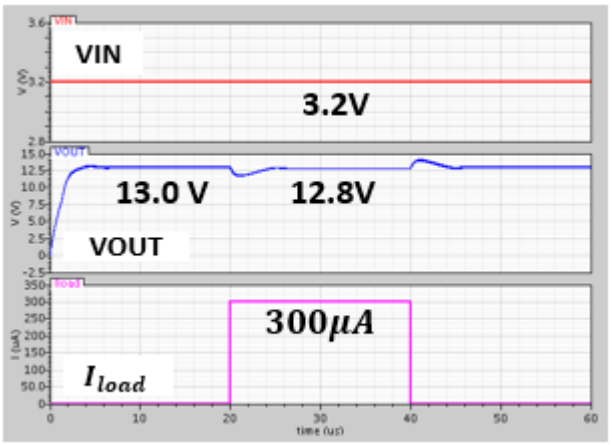


Fig. 4. Circuit schematic of LDO circuit

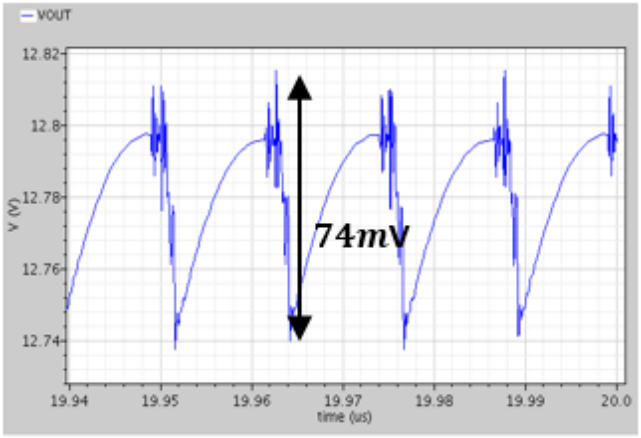
good efficiency but has its limitations in achieving small area as MOSCAP cannot be used as the pumping capacitance in the later stages due to possible breakdown issue. On the other hand, the Cockcroft-Walton architecture [10] in Fig. 2(c) and (d) can employ MOSCAP as its pumping capacitance without reliability issue and thus high integration can be achieved. However, the Cockcroft-Walton architecture is known to have poorer power efficiency in comparison to the Dickson architecture [11].

Figure 3 shows the proposed four-stage charge pump core circuit. A hybrid four-stage topology using two-stage Dickson (Stages 1 and 2) and two-stage Cockcroft-Walton architecture (Stages 3 and 4) is employed which allows to use both metal-insulator-metal (MIM) and MOSCAP as pumping capacitors without reliability issues while achieving relatively good efficiency and small layout area. The capacitors C_1 to C_4 are realized using MOSCAPS with values of 20 pF for C_1 and C_2, and 10 pF for C_3 and C_4. The capacitors C_5 to C_8 are MIM capacitors with 10 pF values. An MIM capacitor of 50 pF is used for the load capacitance. The 3.3-V thick oxide transistors are used as pumping switches in a cross-coupled connection. The core PMOS transistors have dimensions of 18 µm/0.36 µm and NMOS transistors have 10.8 µm/0.36 µm. The respective body terminals of the switches are always connected to the lowest voltage between its drain and source (highest voltage for the PMOS transistors). A dynamic body bias circuit is utilized for this purpose. If the body bias circuit for the upper-left PMOS core transistor is taken as an example, if the source terminal of the upper body bias transistor is at a higher potential than the source terminal of the lower body bias transistor, the lower body bias transistor is turned OFF while the upper body bias transistor is turned ON. This creates a short path between the source terminal of the upper body bias transistor and body terminal of the core PMOS transistor, which ultimately connects the body terminal to the higher potential. The switch implemented using deep n-well NMOS transistor needs two pairs of dynamic body bias transistors to make sure its substrate and n-well are always connected to the correct voltage during operation.

The well-known output voltage equation of a conventional Dickson charge pump circuit is decided by:



(a)



(b)

Fig. 5. (a) Post-layout transient simulation plot of designed charge pump with load current switching between 0 and 300 µA (b) ripple characteristic of the output voltage

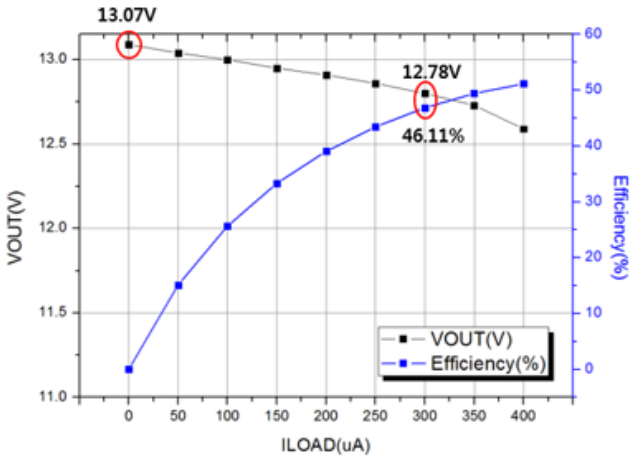
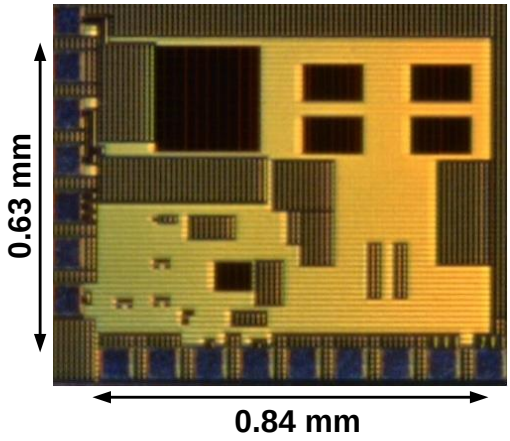
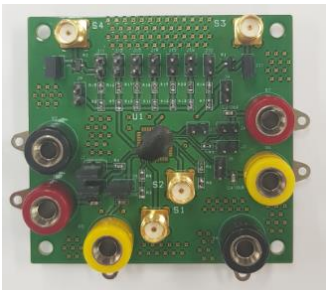


Fig. 6. Post-layout simulated output voltage and power efficiency versus change in load current

$$V_{OUT} = (V_{IN} - V_t) + N \cdot [V_\varphi \frac{C_p}{C_p + C_s} - V_t - \frac{I_L}{f_{osc}(C_p + C_s)}] \quad (1)$$



(a)



(b)

Fig. 7. (a) Chip micrograph and (b) Chip-on-board (COB) packaged IC and measurement PCB

where V_{IN} is the input voltage of charge pump, Vt is the threshold voltage of MOS transistor, VΦ is the pumping clock signal amplitude, f_{OSC} is the pumping clock frequency, Cp is capacitance of pumping capacitor, Cs is the stray capacitance, and I_L is the load current.

For the latched symmetrical charge pump used in this design, eq. (1) can be reduced to [7];

$$V_{OUT} = (N+1)V_{IN} - N\left(\frac{I_L}{2f_{osc}C_p}\right) \quad (2)$$

where both Vt and Cs are assumed to be zero or negligible and the voltage level of VΦ is equal to V_{IN}. It can be understood from equ. (2) that with changing load current, either the clock frequency or the input voltage can be controlled to regulate the output voltage. The disadvantage of controlling the clock frequency is that at very light load condition ($I_L \approx 0$), output regulation may not be achieved as the second part of equ. (2) cancels out at very light load condition. In addition, the efficiency may degrade at heavy load due to increase in pumping frequency due to increase in dynamic switching loss. Thus in this work, input voltage modulation regulation method is chosen to maintain the output voltages with varying load current. Input voltage modulation can achieve good efficiency for the charge pump due to the utilization of a fixed low-frequency clock and advantage with regards to the load regulation performance.

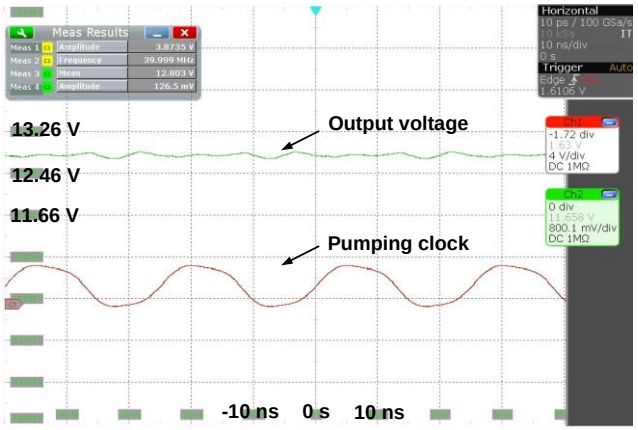


Fig. 8. Measured transient plot of implemented charge pump IC

Figure 4 presents the capacitor-less LDO regulator circuit for sub-charge pump 1. The LDO circuit is comprised of a power transistor M_P, feedback resistors R_{L1} and R_{L2}, an error amplifier, a buffer, and a limiter. The limiter circuit is included to limit the current in M_P, during the beginning stages of the charge pump start-up where it draws a large amount of current. Much attention is given to meeting the stability requirement of the LDO, especially at light load condition at the charge pump output. Miller compensation is used in the error amplifier to meet the stability conditions. The non-overlapping clock generation circuit utilizes NAND gates and chain of inverters to generate CLK1 and CLK2 signals for charge pumping.

Figure 5 shows the post-layout transient simulation of the designed regulated charge pump with switching load current between 0 and 300 µA. It can be observed that due to the regulation loop, the drop in the output voltage is minimal and is maintained at the required output voltage.

Figure 6 shows the post-layout simulated output voltage and power conversion efficiency versus change in load current plot. At 300 µA load current, the efficiency is 46.1% and the maximum efficiency is over 50% at 400 µA load current.

At light current load, the power loss in the charge pump is decided by the bias currents for the LDO/EA circuit and voltage drop at the power transistor of the LDO and pumping switch. When the load current increases, the bias current effect to the efficiency is reduced and the voltage drop in power transistor of LDO will also decrease, which improves the efficiency.

IV. EXPERIMENTAL RESULTS

The proposed charge pump IC is fabricated in a 0.18 µm standard CMOS process. The chip micrograph and photograph of PCB measurement board is shown in Fig. 7(a) and (b), respectively. The core die area is 0.53 mm². The IC is packaged using chip-on-board method and soldered on a two-layer FR4 PCB. The 40 MHz pumping clock is applied externally using an arbitrary waveform generator.

Figure 8 shows the measured output voltage at no load condition. The input voltage of 3.2 V is boosted up to around 12.8 V. However, with heavier load condition, the regulation performance is observed to be degraded compared to the simulation results. Some additional leakage current within

Table I. Performance Summary

Parameter	This work	[11]	[12]
Number of stages	4	4, 6	3, 5
Input voltage (V)	3.2	1	1.8
Output voltage (V)	12.8	3-6	5-8.5
Ripple voltage (V)	74 m*	40 m	-
Pumping cap. (F)	10 p/20 p	6 p	2.5 p
Load cap. (F)	50 p	54 p	30 p
Max. load current (A)	300 µ	240 µ	400 µ
Switching freq. (Hz)	40 M	10k-20M	100 M
Power Efficiency (%) @ Vout, max	46.1 @ 300 µA*	52 @ 240 µA	46 @ 200 µA
Load regulation (V/mA)	0.77*	2.78	3.75
Area (mm^2)	0.53	0.5	1.3
Process	180 nm CMOS	180 nm CMOS	180 nm CMOS

*Post-sim. results

the IC and/or PCB is suspected to have caused this degradation in performance. Improved layout and PCB design in the future should lessen the degradation. Table I presents the performance summary of this work (post-layout simulation values are used for comparison) and compares to previously reported charge pump ICs with integrated pumping and load capacitance. As the application and requirements of the charge pumps are all different, a fair comparison is difficult. In summary, this work provides a HV output with good load regulation performance with small area and comparable power efficiency.

V. CONCLUSIONS

A high-voltage hybrid-core charge pump IC with input voltage modulated regulation is proposed for neural stimulation applications using 180 nm standard CMOS process. The proposed IC outputs 12.8 V from a 3.2 V input, supports load currents up to 300 µA, and achieves 0.77 V/mA load regulation performance and 46.1 % power efficiency.

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