Novel test patterns for analog/mixed signal device reliability and electrical parameter extraction

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Abstract **- In this paper, we proposed four test patterns for monitoring of technology and extracting device parameter by using Magnachip/SK hynix 0.18μm analog/mixed signal technology. Firstly, to evaluate interface quality of ultra-thin gate oxide transistor, On-Chip Charge Pumping (OCCP) test pattern was designed. OCCP test pattern consists of Ring Oscillator (RO) and Level shifter module and its maximum frequency is about 500 MHz. But, unfortunately actual OCCP test pattern did not operate except for RO test pattern. Maybe it would be incorrect design of buffer size. So, OCCP design will be modified next Multi-Project Wafer (MPW). Secondly, to estimate photon injection effect, we propose new MOSFET layout structure for high efficient photon injection. Conventional MOSFET has many layers such as ILD, IMD, metal etc. But, our proposed test patterns are designed without these things to analyze optical performance. Thirdly, to evaluate sheet resistance, we proposed kelvin measurement structure. The proposed structure needs less contact pad and area. This test structure expected to reduce at least 40% area compared with conventional kelvin structure. So the exact phonon effects are difficult to estimate. The proposed test pattern has optical path to enhance photon injection efficiency and can help us to measure and analyze optical these effects easily. Fourthly, to estimate the analog performance degradation due to Hot Carrier Injection (HCI), Negative Bias Temperature Instability (NBTI) and Time Dependent Dielectric Breakdown (TDDB), discrete MOSFETs were proposed. Finally, to extract Effective Schottky Barrier Height (ESBH), pn junction diode structures are designed by using CMOS process. With this patterns, we measured ESBH by using activation energy extraction method. In this time, activation energy was measured range from 0.0009 eV to 0.0375 eV.**

I. INTRODUCTION

As semiconductor technology evolves, non-ideal effects have occurred in analog circuits such as transient charging effect, leakage current, self-heating, etc. So, to diagnose product functionality, reliability in details, more various and novel test patterns have been gradually required. Although analog parameter is very important and is needed for extracting device parameter for analog designer, most of the research focused on digital parameters only. So the analog parameter degradation characteristics need to be analyzed. And since the low frequency noise characteristics are one of the key factors in analog circuit, these analog parameter is related to interface state quality. But as the scaling down of the device, verifying interface quality of single device is getting difficult. Firstly, we designed OCCP test pattern. Charge pumping technique is a well-known method to characterize the interface state, and energy distribution and capture cross-section of interface state in MOSFETs. However, as the minimum feature size of device shrinks down, conventional charge pumping method is no longer effective because of excessively increased gate direct tunneling current [1-5]. Moreover, aggressively reduced effective-channel length can make it more difficult. Therefore, increase of pulse frequency is needed for evaluate these transistors. It is not conducted by external pulse generator, because in high frequency pulses applied to DUT by external pulse generator can be distorted a lot due to the parasitic capacitance and resistance of metal pads, probe line and interconnect line. So it is needed to be designed in on-chip overall. For this reason, we designed OCCP test patterns and it will be a powerful tool for evaluating state of the art device.

Secondly, we designed Optical charge pumping (OCP) test pattern. Optical charge pumping technique is very powerful tool for analyzing of gate oxide quality. However, to measurement optical charge pumping (OCP), Optical stress effects on the gate oxide and photon effects on Random Telegraph Signal (RTS) noise, optical path is essential to arrive perfectly at Gate oxide to Silicon interface [6]. However, conventional MOSFET structure has many metal lines above gate, source, drain. These metal lines forbid photons to arrive perfectly at gate oxide to silicon interface. So these obstacles should be far from optical path. To solve these problems and to inject photon high efficiently, New MOSFET layout is needed which does not have metal lines above gate, source, drain. We call these layout as Optical Measurement MOSFET Layout (OMML).

Thirdly, we designed modified kelvin measurement test pattern. As the integration technology improving, not only the active devices are shrink down, but also the passive devices.

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Therefore, measuring the passive component is getting difficult because of the parasitic effect such as cable capacitance, resistance, leakage current, coupling effect, etc. For the resistor, there is Kelvin measurement method. Kelvin measurement is also known as four-terminal measurement. This method is an impedance measuring technique to measure accurate impedance than two-terminal measurement method. The conventional kelvin measurement structure is shown in Fig. 1. The current is supplied through force connection and then a pair of sense connections are measuring the voltage across the resistor.

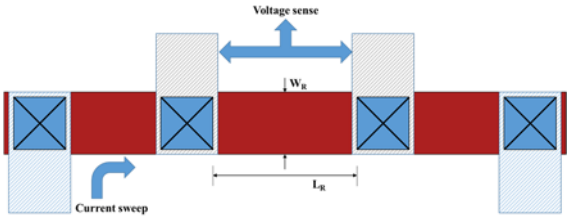


Fig. 1. Kelvin measurement concept.

Since, there is no current flow on force connection, the accurate impedance can be measured in sense connection. But, if there are many resistors to measure the impedance, we need significant space for kelvin measurement pattern. So we propose a novel structure for reducing the area of measurement test patterns.

Fourthly, the reliability issues such as hot carrier, NBTI, TDDB, and so on of MOSFETs have gained attention for a long time and the efforts to enhance the lifetime and performance have continued [7-16]. This attention and efforts lead to success the continued MOSFET scaling down to 14 nm node or beyond. Because the MOSFET scaling down will continue according to technological innovation, the study also will continue to mitigate the reliability degradation and to improve the transistor lifetime.

Finally, we proposed test patterns for extracting ESBH. With the device scaled down, the relative contribution of contact resistance increases significantly [17]. This can lead problem such as RC delay or decreased gain [18]. Today, it has been reported that contact resistance between metal and source/drain is closely related to an ESBH [19]. But extract of ESBH between heavy doped silicon and metal using calculation method like I-V measurement, Norde measurement, Cheng`s measurement is not accurate because it is performed like ohmic contact. So I-V measurement in low temperature condition is important to extract accuracy ESBH value.

In this paper, we proposed four test patterns to evaluate various analog parameter. Each pattern is valuable things to extract analog parameter exactly.

II. EXPERIMENTS AND DISCUSSION

Fig. 2 shows overall layout of test patterns. Our test pattern has many test pads contrary to general MPW chips. It was organized by sub-themes for each test pattern. Each test pattern was described by four sub section in details.

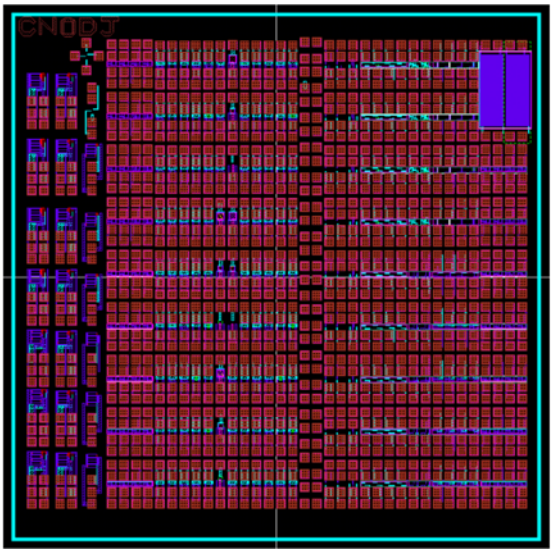


Fig. 2. Test pattern layout to evaluate analog parameter.

A. On-chip charge pumping test pattern for evaluating ultra-thin gate oxide transistor

Our designed OCCP test pattern mainly consists of RO, level shifter, and transmission gate blocks as shown in Fig. 3 and each block is described in Fig. 4. In case of RO, each blocks are connected by parallel for generating diverse pulse. First, RO generates a high frequency pulse. Then level shifter which can control the peak to peak voltage of high frequency pulse and the output is applied to the gate of MOSFET through transmission gate. High frequency pulse is applied to gate of DUT transistor only when the transmission gate is ON [20].

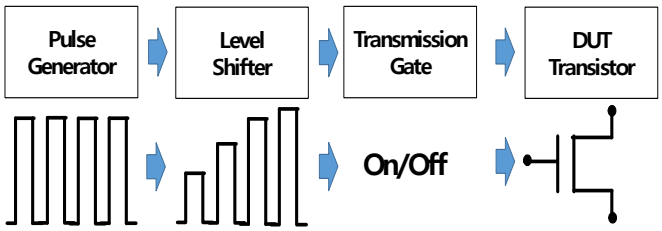
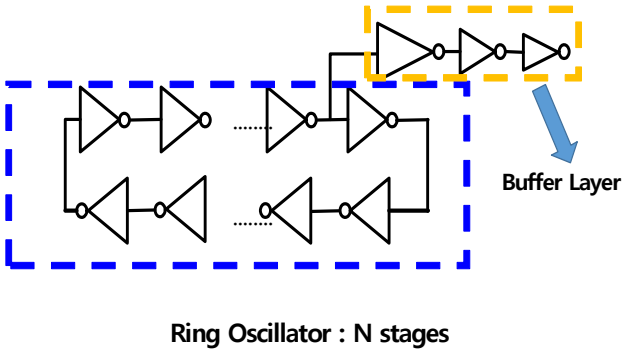


Fig. 3. Design concept of OCCP circuit.



(a)

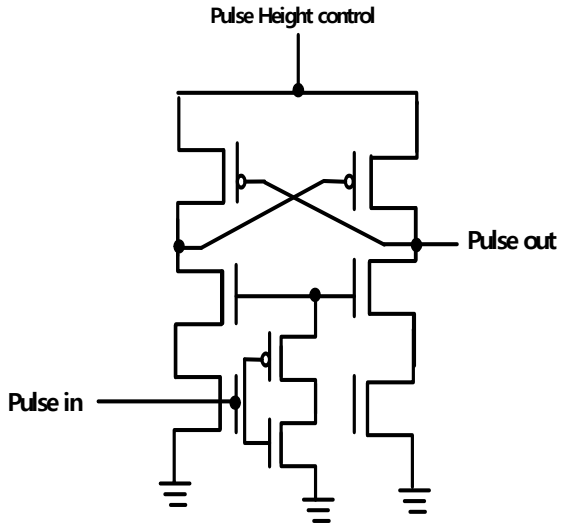


Fig. 4. On-chip charge pumping test pattern blocks. (a) Ring oscillator (b) Level shifter

In addition, because gate delay is very important issue for exact measurement of OCCP, to find out gate delay of transistor and optimize OCCP test pattern performance, RO patterns were also designed by a transistor width and length. It is very important to know a gate delay, because it is related to pulse frequency. Split of test patterns is described in Table 1.

TABLE 1.
Designed RO test pattern for evaluating gate delay.

Test pattern name	Transistor size W/L*[um/um]
RO1	0.18/0.18
RO3	0.72/0.18
RO4	10/0.18

*It is the nmos transistor size. In case of the pmos transistor, width is twice larger than the nmos.

Fig. 5 shows our completed On-chip charge pumping test pattern blocks. Using this blocks, interface state density could be extracted in ultra-thin oxide transistor pattern.

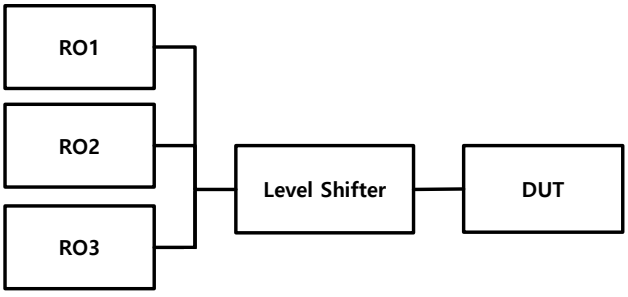


Fig. 5. Completed On-chip charge pumping test pattern blocks.

Unfortunately, actual OCCP circuit did not operate and we cannot extract interface trap density. But, to analyze each OCCP circuit component, we split into RO and Level shifter and RO circuit were operated and we extracted gate delay parameter. Fig. 6 shows gate delay parameter according to width/length splits.

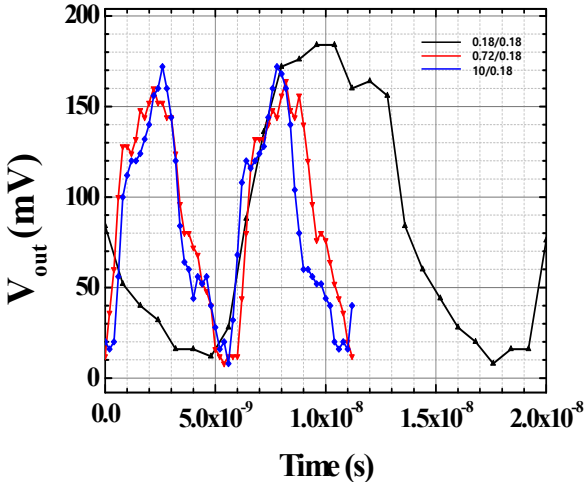


Fig. 6. Waveform of RO test pattern for evaluating gate delay parameter.

By using this test pattern circuit, we can extract analog parameter gate delay for designing analog circuit. In the near future, we will design OCCP circuit again.

B. Test pattern for measurement of OCP

To Measure OCP, we have designed metal lines far from active region not to block optical path. Fig. 7 shows OMML cross section view and Fig. 8 shows OMML above section view. Fig. 9 shows side section view. As these figures show, metal1 and via1 are located far from source, gate, drain region. Additional metals are also located above far from active region. In conclusion, we can measure and analyze optical effects and optical charge pumping by using this test patterns.

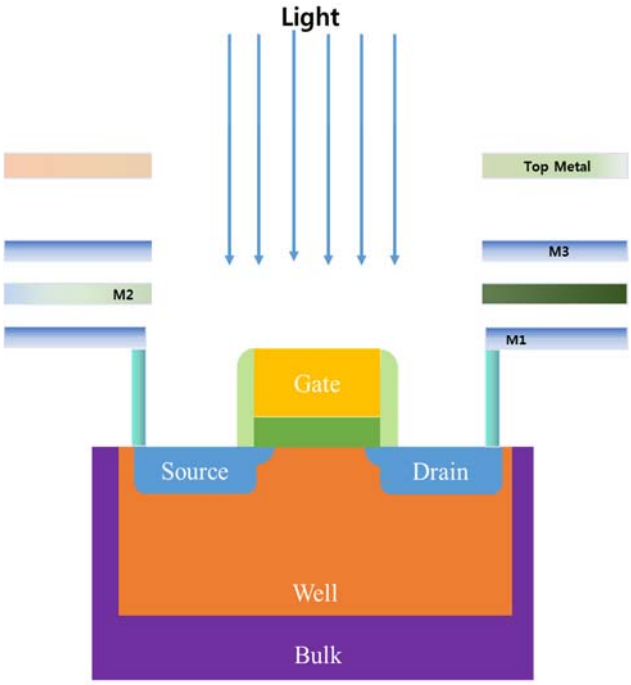


Fig. 7. OMML cross section view.

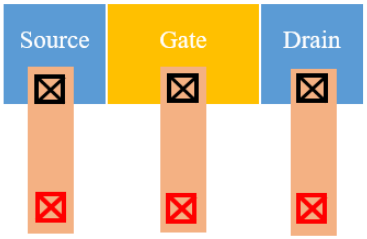


Fig. 8. Top view of OMML structure.

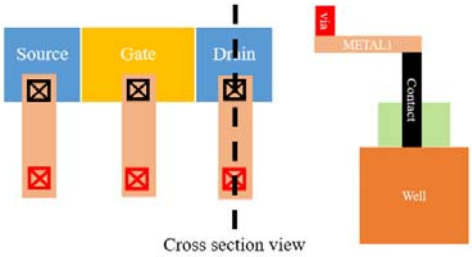


Fig. 9. Side section view of OMML.

The key point is the location of metal line above active region. Conventional MOSFET has contact and many metal lines above active region to reduce parasitic resistance. Metal lines can also reflect photon. So photon cannot inject into active region perfectly. We can measure and analyze optical effect by using conventional MOSFET layout. However, OMML has no metal lines above active region. They are far from active region not to prohibit photon injection.

To achieve our measurement and analysis, we need gate length, gate width and gate oxide thickness splits because RTS noise depends on the size of MOSFET and optical stress effect on gate oxide also depends on oxide thickness split. Besides we want to measure optical charge pumping in various size of MOSFET.

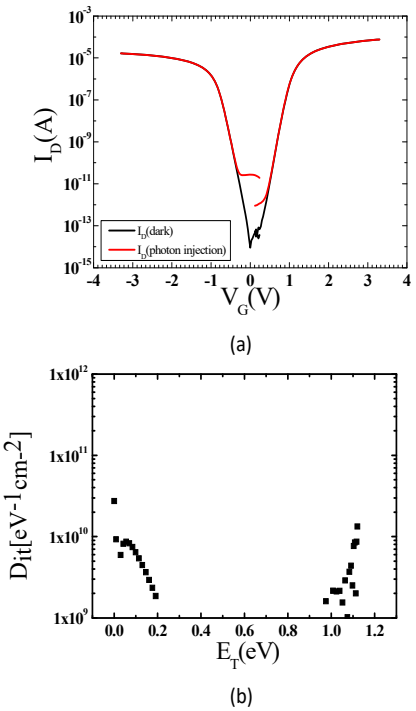


Fig. 10. OMML cross section view.

Fig. 10 shows actual optical charge pumping measurement result. Using this test pattern, we extracted interface state density.

C. A novel test structure for Kelvin measurement

Fig. 11 shows proposed Kelvin measurement structures for 3 resistors of different width. If there are many resistors to measure the impedance, we need significant space for kelvin measurement pattern. So we propose a novel structure for reducing the area of measurement test pattern.

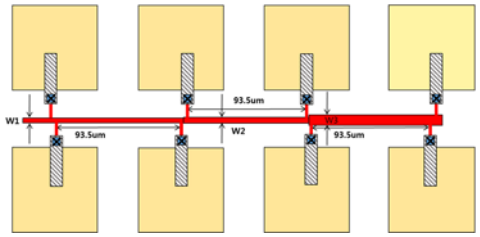


Fig. 11. Proposed Kelvin measurement structure for 3 resistors of different width.

If we design three conventional resistors for kelvin measurement, we need 12 contact pad and space. However, the proposed structure only needs 8 contact pad and much less space. This test structure can reduce at least 40% area compared with conventional kelvin structure.

D. Analog/Mixed signal MOSFET's reliability and LFN noise test pattern

To measure the gate length and width dependency of reliability or sometimes 1/f noise, charge pumping, capacitance, and so on, the gate length is split by 0.18, 0.25, 0.35, 0.5, and 1 μm with gate width of 10 and 20 μm (Table 2.) and the gate width split by 0.5, 1, 5, 10 and 20 μm with gate length of 0.35 and 0.5 μm (Table 3.). And thick devices are operated in 3.3 V and thin devices are operated in 1.2 V. In order to evaluate reliability characteristics, source, drain, gate and body must be separated. Especially, the gate must be separated to induce the stress and the body must be separated for the charge pumping measurement and body current sensing. In other word, all of transistors need to have N well in case of PMOS and P well in case of NMOS. To minimize the test results variability between transistors, we need 5 transistors per 1 die.

TABLE 2.
Transistor Gate length split for reliability evaluation.

Transistor name	Transistor size W/L[um/um]
Tr1-1	20/0.18
Tr1-2	20/0.25
Tr1-3	20/0.35
Tr1-4	20/0.5
Tr1-5	20/1.0
Tr2-1	10/0.18
Tr2-2	10/0.25
Tr2-3	10/0.35
Tr2-4	10/0.5
Tr2-5	10/1.0

TABLE 3.
Transistor Gate width split for reliability evaluation.

Transistor name	Transistor size W/L[um/um]
Tr3-1	0.5/0.35
Tr3-2	1/0.35
Tr3-3	5/0.35
Tr3-4	10/0.35
Tr3-5	20/0.35
Tr4-1	0.5/0.5
Tr4-2	1/0.5
Tr4-3	5/0.5
Tr4-4	10/0.5
Tr4-5	20/0.5

To test the TDDB, the source-drain tied MOSFETs called GOI pattern are needed. Each transistor is described in Table 4. To minimize the test results variability between transistors, we need 15 transistors per die.

TABLE 4.
Transistor GOI pattern split.

Transistor name	Transistor size W/L[um/um]
Tr5	20/20
Tr6	50/50

As the scaling down of MOSFETs continues, the reliability issue will be studied more aggressively. The suggested MOSFETs in table 2, 3, 4 will be used to analyze the hot carrier, NBTI, TDDB degradation mechanism of analog performance characteristics. Also we can use the low frequency noise measurement technique, to evaluate gate oxide bulk trap characteristics and the relationship with stress induced degradation.

E. Test patterns for extracting Schottky barrier height by using low temperature measurement

To study accurate ESBH barrier height mechanism, n+/p and p+/n, $CoSi_2$/n-Si, $CoSi_2$/p-Si diode and n, p resistor patterns are measured respectively. Before measuring the diode and resistor, ESBH and resistance will extract by calculation. After extraction of ESBH and resistance by calculation, patterns will be measured in low temperature vacuum chamber using four-wire measurement to extract the more accurate I-V value because of four-wire measurement to remove any parasitic resistance. After measurement of I-V, we used currents under reverse bias for extraction of the SBH [21]. According to the thermionic emission theory, temperature dependence of the reverse current is followed using equation (1)

$$\ln\left(\frac{I_R}{T^2}\right) = \ln(AA^{**}) - \frac{q\Phi_B^n}{kT} \qquad (1)$$

Where A is the diode area, $A^{**}$is the effective Richardson constant, k is the Boltzmann constant, q is the electronic charge, and T is temperature. Fig. 12 shows method to extract SBH from plot of I_R/T^2 versus 1000/T. Slope can be obtained by linear fitting.

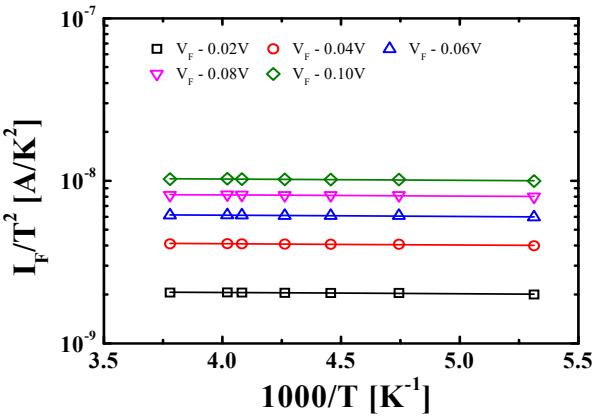


Fig. 12. Activation energy plots to extract ESBH.

Table 5. shows actual results of ESBH of our designed test patterns. Activation energy was measured range from 0.0009 eV to 0.0375 eV.

TABLE 5.
Extracted ESBH by our designed patterns.

Bias voltage [V]	ESBH [eV]
0.02	0.000904
0.04	0.001856
0.06	0.002810
0.08	0.003750
0.10	0.004759

IV. CONCLUSIONS

To evaluate analog circuit performance, five test patterns were designed and measured by electrical characteristics. Although OCCP patterns did not operate, RO circuit were operated and we extracted gate delay parameter. Using the OCCP pattern, more reliable charge pumping measurement could be achieved. And proposed kelvin pattern could reduce the area about 40% than conventional structure. And for the phonon effect analysis, in our previous measurement, there were limits that we could not solve even though we change photon injection angle to enhance photon injection efficiency and photon intensity. So we must need the test pattern for our measurement. And analog performance degradation can be evaluated through the test pattern we proposed. It was meaningful because the analog device performance degradation not yet been analyzed in depth.

ACKNOWLEDGMENT

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