A 33.3% Power Efficiency RF Energy Harvester with -25 dBm Sensitivity using Threshold Compensation Scheme

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***Abstract* - This paper presents an ultra-low power RF-DC voltage multiplier using auxiliary transistors block to dynamically control the threshold voltage of the main chain transistors. The proposed scheme enhances the forward conduction current and reduces the reverse current by controlling the gate to source voltage of the main chain transistors. The proposed 5-stage scheme attains maximum post-layout simulated power conversion efficiency (PCE) of 33.3% at -16dBm input level and delivers 2.63 V output DC voltage to 1MΩ load. The proposed RF-DC voltage multiplier has been designed in a standard 180 nm CMOS technology.**

I. INTRODUCTION

For more than a decade, energy harvesting from ambient environment has been attracting a great deal of interest in powering up the electronic devices and has become a favorable substitute for the battery. The RF energy harvesting is one of the most popular methods of extracting power from ambient environment to supply the wearable electronic devices, internet of things (IoT), wireless sensor networks (WSN) and biomedical implantable devices [1]. Usually the signal strength of incoming RF signal is limited to turn on a rectification device so we need an efficient RF to DC conversion circuit to overcome this challenge.

Fig. 1 shows a basic block diagram of RF energy harvester. The incident RF signal from the antenna feeds to matching network which maximizes the power transfer from the antenna to the rectifier circuit. The rectifier circuit rectifies the input RF power and converts it to DC output power. The DC output voltage is stored in the storage device and supplies to the required load.

The major challenge in RF rectifier circuit design is to minimize the threshold voltage when transistors are forward biased to allow the current flow in the forward direction and maximizes the threshold voltage when transistors are reversed biased to prevent the leakage current. To achieve the maximum rectifier's efficiency, energy losses introduced by the threshold voltage and reverse current must be reduced.

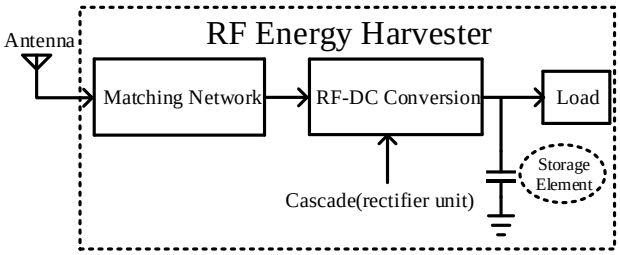

Fig. 1. Block diagram of RF Energy Harvesting

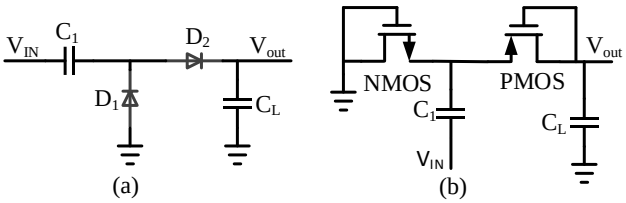

Fig. 2. Rectifier unit (a) diode-based voltage doubler (b) diode connected MOS based voltage doubler

Power conversion efficiency (PCE) determines the performance of the rectifier unit which is the ratio of the power delivered to the load to the input RF power. Mathematically,

$$PCE = (P_{out,\,forward} - P_{leakage}) \div P_{input} \quad (1)$$

where P_{input} is the RF input power, $P_{out,forward}$ is the output power and $P_{leakage}$ is the power lost due to leakage current.

A lot of solutions have been presented in order to reduce the threshold voltage and reverse leakage current of the rectification devices. Technology based approach uses schottky diodes [2] which have low threshold voltage and low turn-on voltage but main drawback of this approach is additional fabrication steps and production cost. In [3], self-biasing technique is used with DC biasing voltage which results in more power consumption and additional area. In [4], NMOS transistors with body connected to ground result in body effect which ultimately increases threshold voltage of the transistors. Differential circuits discussed in [5, 6] have cross coupled bridge configurations which require differential antenna. In [7], floating well technique is used to control body terminal of the transistors.

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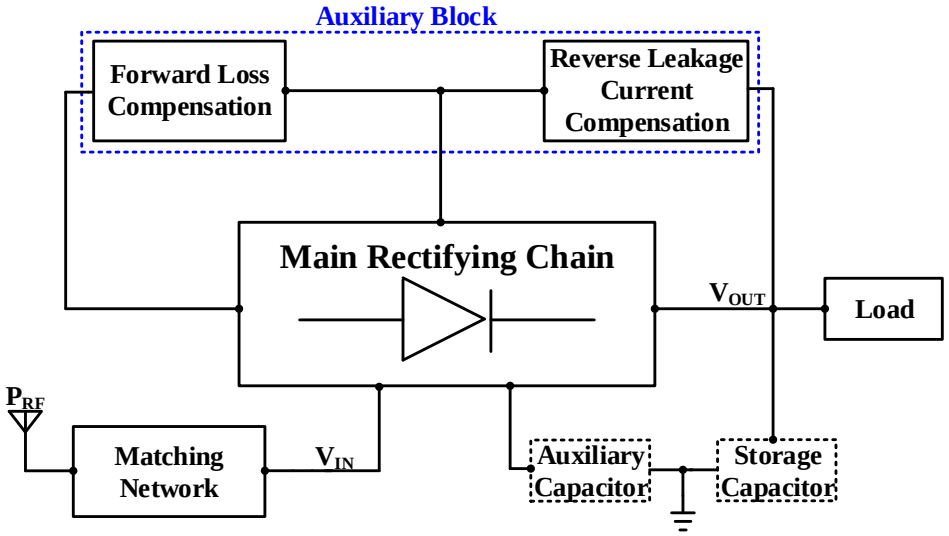

Fig. 3. Block diagram of the proposed RF-DC voltage multiplier using auxiliary block scheme

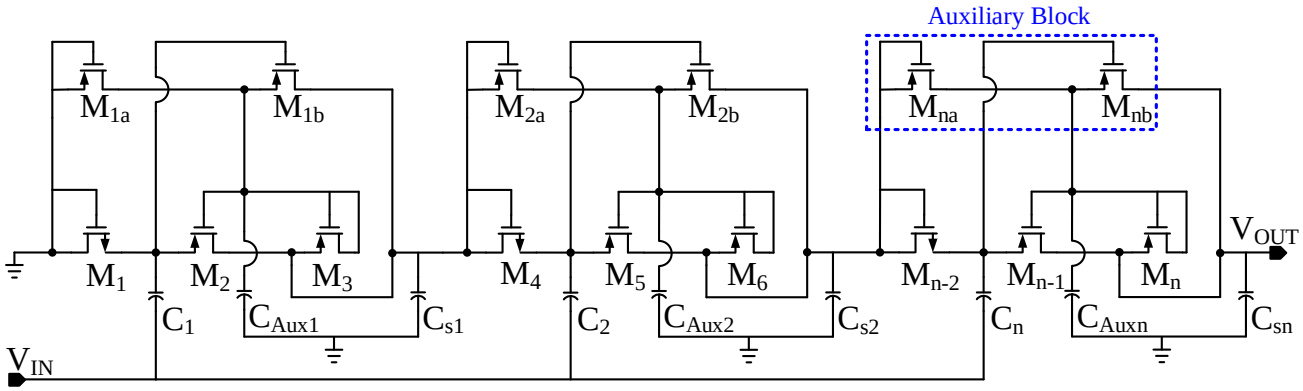

Fig. 4. Circuit diagram of the proposed RF-DC voltage multiplier using auxiliary block scheme

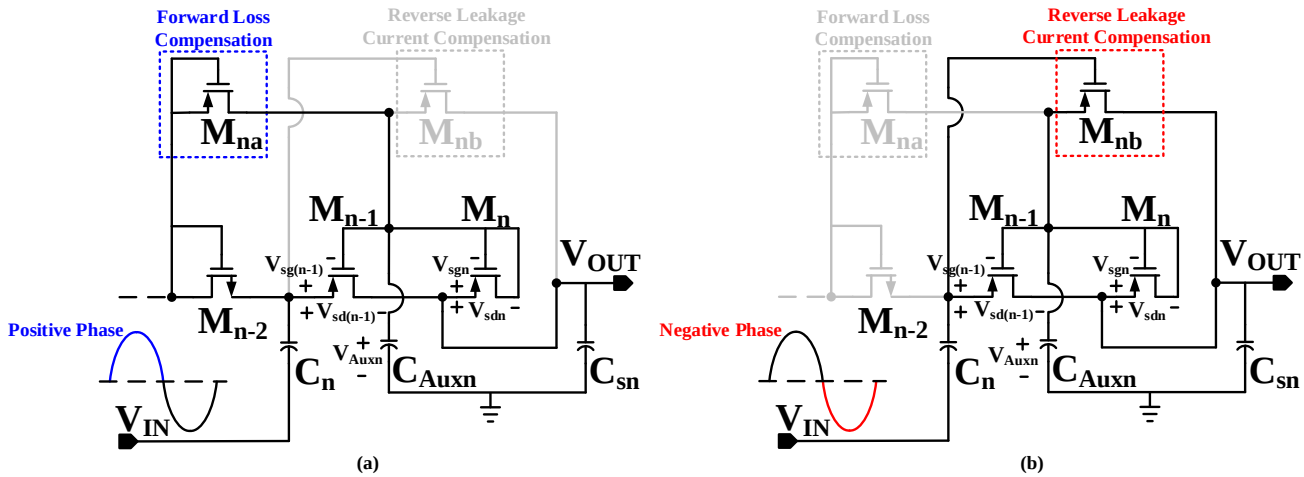

Fig. 5. Operation of the proposed scheme during (a) Positive Phase and (b) Negative Phase

The drawback of this technique results in undesirable substrate current. Active circuit technique [8] to reduce threshold voltage of rectifying device utilizes external power supply resulting in increased cost and maintenance. Multi-level threshold-compensation [9] decreases the threshold voltage of the transistors but leakage current also increases which degrades the efficiency. To control the reverse leakage current, the author in [10] used high speed comparator. But the use of high speed comparator increases power consumption and make it less useful for low-frequency application. Many techniques such as External Vth cancellation (EVC) [11], Internal Vth

cancellation (IVC) [12] and Self-Vth cancellation (SVC) [13] are used to reduce the threshold voltage of the MOS transistor in the rectifier circuit.

In this paper an efficient RF-DC voltage multiplier using auxiliary transistors block for ultra-low RF input power level is proposed. The proposed scheme enhances the PCE by reducing the voltage drop across the forward-biased transistors to increase the conduction current and increases the threshold voltage of the reverse-biased transistors to prevent the leakage current.

This paper is organized as follows. Section II presents the overview of the prior work. Section III provides the proposed scheme. Section IV discusses the results of proposed scheme. Comparison with the previous state-of-the-art works is made in Section V. Finally, conclusion is discussed in Section VI.

II. OVERVIEW OF PRIOR WORK

Threshold voltage of a rectifying device significantly affects the performance of the RF energy harvesting system. A low threshold voltage rectifying device is necessary for the operation of RF-DC converter to efficiently rectify low RF power to DC power. There are two types of techniques are being used to reduce the threshold voltage and leakage current in the rectifier circuit (1) technology-based and (2) circuit-level technology.

Fig. 2(a) shows the diode-based voltage doubler. The diodes can also be implemented by connecting drain and gate terminal of MOS transistor together as shown in Fig. 2(b) which keeps the transistor always in the saturation region for forward-biased connection. The voltage doubler rectifies the AC voltage to DC voltage. Each of the two transistors in the voltage doubler conducts only during one half of the input cycle. The output voltage of the voltage double can be expressed as:

$$V_{out} = 2V_p - V_{th1} - V_{th2} \quad (2)$$

where V_p is the peak amplitude of input RF signal, V_{th1} and V_{th2} are the threshold voltages of NMOS and PMOS transistors respectively.

The output voltage of the voltage doubler can become double of the input voltage only when the threshold voltage of the two transistors becomes zero. However, if the threshold voltage is reduced it introduces the reverse leakage current during the negative half cycle which results in the degradation of the power conversion efficiency (PCE).

III. PROPOSED THRESHOLD VOLTAGE COMPENSATION SCHEME

Fig. 3 shows block diagram of the proposed RF-DC voltage multiplier scheme using auxiliary block. Fig. 4 shows circuit diagram of the proposed voltage multiplier using auxiliary block. The proposed auxiliary block consists of two PMOS transistors in each stage to dynamically control the gate to source voltage of the main chain transistors. The auxiliary block uses minimum number of transistors in order to avoid additional power consumption. Consider the nth stage of Fig. 4 which is well-defined in Fig. 5. The auxiliary block transistors M_{na} and M_{nb} compensate forward-loss and reverse leakage-loss in the main rectification chain during positive and negative half cycle of the input RF signal respectively. Therefore, this process reduces the voltage drop across the forward-biased transistors in order to increase the conduction current and increases the threshold voltage of the reverse-biased transistors to prevent reverse current. The main rectification chain consists of one NMOS transistor and two PMOS transistors in each stage for the rectification of the input RF power. The gates of both the PMOS transistors are connected together to nullify the threshold effect of each other. The use of auxiliary capacitor C_{Auxn} is to preserve the charge which is usually lost during reverse-conduction. The proposed scheme is cascaded in series to improve the power conversion efficiency required for ultra-low power RF energy harvesting applications.

Consider the last stage i.e. nth stage of the proposed scheme. By applying Kirchhoff's voltage law (KVL) in Fig. 5.

$$V_{IN} = V_{sd\,(n-1)} + V_{OUT} \quad (3)$$

$$V_{OUT} = V_{Auxn} + V_{sdn} \quad (4)$$

By re-arranging (1) and (2), we get:

$$V_{OUT} = \frac{1}{2}\,(V_{IN} - V_{sd\,(n-1)} + V_{sdn} + V_{Auxn}) \quad (5)$$

where V_{IN} is the peak amplitude of input RF signal, $V_{sd\,(n-1)}$ and V_{sd} are the voltage drop across M_{n-1} and M_n transistors respectively and V_{Auxn} is the voltage across capacitor C_{Auxn}.

Similarly,

$$V_{IN} = V_{sg\,(n-1)} + V_{Auxn} \quad (6)$$

By putting value of V_{IN} from (6) into (3), we get:

$$V_{OUT} = -V_{sd\,(n-1)} + V_{sg\,(n-1)} + V_{Auxn} \quad (7)$$

Similarly,

$$V_{OUT} = V_{sgn} + V_{Auxn} \quad (8)$$

By subtracting (7) from (8) gives:

$$V_{sd\,(n-1)} = V_{sg\,(n-1)} - V_{sgn} \quad (9)$$

The increase in the output voltage makes the gate-source voltage of M_n transistor increases continuously. This will help the transistor M_{n-1} to enter in the saturation region when gate-source voltage of the M_n transistor becomes equal to threshold voltage. Hence, we can rewrite (5) as:

$$V_{OUT} = \frac{1}{2}\,(V_{IN} - V_{th\,(Mn-1)} + V_{th\,(Mn)} + V_{Auxn}) \quad (10)$$

From (10), we can say that the proposed scheme is capable of minimizing the effect of threshold voltage of the transistors

in the main rectification chain. This increases the harvested power and improves the power conversion efficiency.

Fig. 5 shows the operation of the proposed scheme during positive and negative phase of the RF input signal. During the positive half cycle, M_{na} transistor in the auxiliary block keeps the transistors M_{n-1} and M_n back-compensated to reduce voltage drop across these transistors in the main rectification chain. This increases the forward conduction current and enhances the power transfer to improve the power conversion efficiency. During the negative half cycle, the transistor M_{nb} in the auxiliary block keeps the gate-source voltage of transistors M_n and M_{n-1} to zero to reduce the reverse leakage current.

IV. RESULTS AND DISCUSSION

Fig. 6 shows the layout of the proposed 5-stage RF-DC voltage multiplier using auxiliary block scheme. The active die area of the proposed 5-stage voltage multiplier is (213µm x 213µm). The total value of the capacitance, which is the sum of input capacitance, auxiliary capacitance and storage capacitance, is 54.9pF. Fig. 7 shows the simulated results of the proposed scheme in a standard 180 nm CMOS technology. Fig. 7(a) shows the efficiency versus input power level (-25dBm to -10dBm) graph for different rectifier stages by keeping the load of 1MΩ. Different No. of stages show different efficiency performance versus input power range from -25dBm to -10dBm. The proposed 5-stage RF-DC voltage multiplier achieves maximum power conversion efficiency (PCE) of 33.3% at -16dBm input power level. The PCE of the proposed scheme gradually increases from (-25dBm to -12dBm) input power level and then starts decreasing. From this graph, it can be concluded that the proposed scheme is suitable for low input power level. Fig. 7(b) shows graph of output DC voltage of different stages versus input power level. It can be seen from the graph that the output DC voltage increases with the increase in number of stages and vice versa. The proposed 5-stage RF-DC voltage multiplier produces an output DC voltage of 2.63V to 1MΩ load.

V. COMPARISON WITH PREVIOUS WORKS

Table I compares the performance of the proposed RF-DC voltage multiplier with the prior state-of-the-art works. The proposed scheme is designed in a standard 180nm CMOS technology. The active die area of the proposed 5-stage voltage multiplier is (213µm x 213µm). The RF input power level ranges from -25dBm to -10dBm to check the power conversion efficiency (PCE) of different stages (i.e. from 1 to 8) of the proposed scheme at 900 MHZ frequency. Different no. of stages show different efficiency performance vs RF input power level from -25dBm to -10dBm. The proposed 5-stage RF-DC voltage multiplier achieves the post-layout simulated PCE of 33.3% at -16dBm input power level and delivers an output DC voltage of 2.63V to 1MΩ load.

VI. CONCLUSIONS

The paper presents an ultra-low power RF-DC voltage multiplier using auxiliary transistors block to dynamically control the threshold voltage of the main chain transistors. During positive half cycle, the proposed circuit increases the conduction current by reducing the threshold voltage of the forward-biased transistors. Similarly, during negative half cycle, the proposed circuit prevents the flow of leakage current by increasing the threshold voltage of the reverse-biased transistors. The proposed scheme attains maximum post-layout simulated power conversion efficiency (PCE) of 33.3% at input power level of -16dBm and feeds output DC voltage of 2.63V to 1MΩ load. The proposed RF-DC voltage multiplier has been designed in a standard 180 nm CMOS technology.

ACKNOWLEDGMENT

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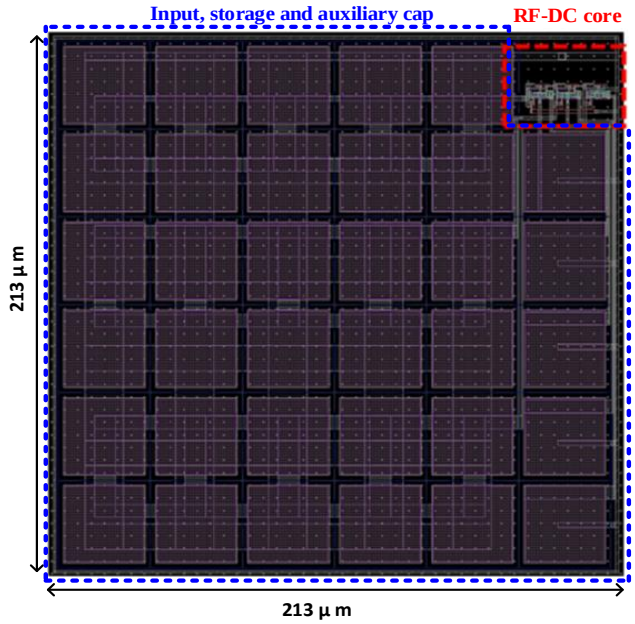

Fig. 6. Layout of the proposed 5-stage voltage multiplier

REFERENCES

[1] K. Finkenzeller, *Fundamental And Applications In Contactless Smart Cards And Identification*, RFID Handbook, Wiley, 2003.

[2] U. Karthaus; M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-µW minimum RF input power," *Journal of Solid-State Circuits, IEEE*, vol. 38, no. 10, pp. 1602-1608, Oct 2003.

[3] B. Li; X. Shao; N. Shahan; N. Goldsman, T. Salter; G. Metze, "An antenna co-design dual band RF energy harvester," *Transactions on Circuits and System. I, IEEE*, vol. 60, no. 12, pp. 3256-3266, Dec 2013.

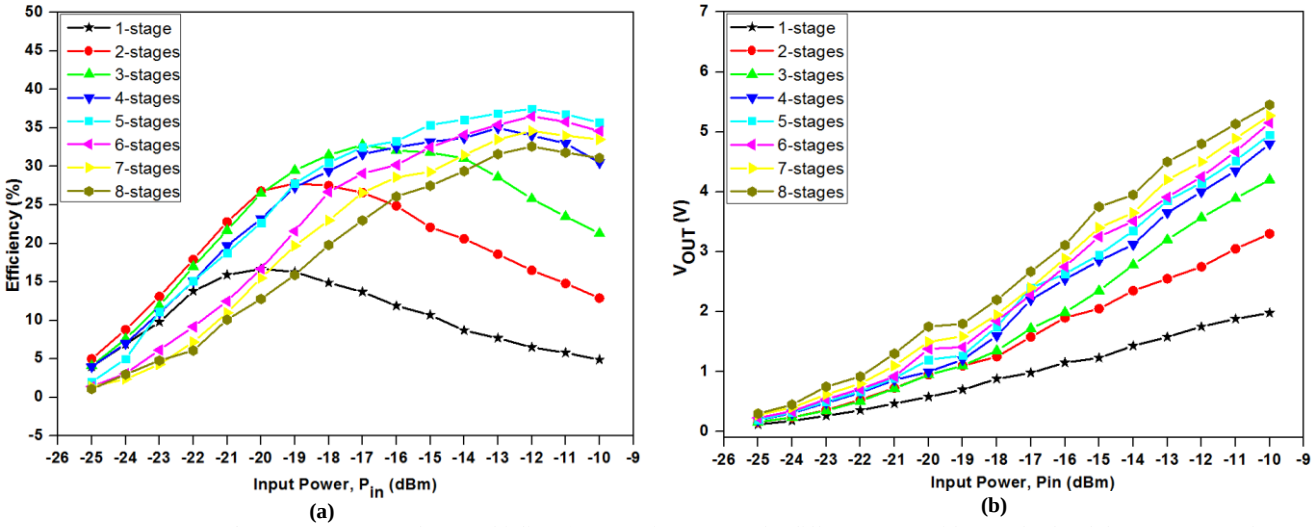

Fig. 7. Simulation results of proposed RF-DC voltage multiplier (a) PCE vs input power for different stages with 1MΩ load and (b) Output DC voltage vs input power for different stages with 1MΩ load

TABLE I
Performance comparison with the prior state-of-the-art works

Parameters	This work*	[9]	[6]	[3]	[11]	[12]	[13]
Technology(nm)	180	130	130	130	135	180	135
Input (dBm)	-16	-16.8	-16	-19.3	57	-8	-9.9
Load (MΩ)	1	1	-	1.5	-	0.01	-
Output DC (V)	2.63	2.2	2	1.15	-	-	-
PCE (%)	33.3	22.6	10	9.1	36.6	35	29
Frequency (MHz)	900	915	868	900	860-960	433	860-960
Voltage sensitivity: 1 V for 1 MΩ load	-21dBm	-21.6dBm	-16dBm	-19.3	-	-	-

*Post-Layout simulation results are presented

[4] J. Shin; I. Y. Chung; Y. J. Park; H. S. Min; "A new charge pump without degradation in threshold voltage due to body effect," *Journal of Solid-State Circuits, IEEE*, vol. 35, no. 8, pp. 1227-1230, Aug 2000.

[5] M. Stoopman; S. Keyroz; H. J. Visser; K. Philips; W. Serdin, "Co-design of a CMOS rectifier and small loop antenna for highly sensitive RF energy harvesting," *Journal of Solid-State Circuits, IEEE*, vol. 49, no. 3, pp. 622-634, Feb 2014.

[6] S. Scorcioni; L. Larcher; A. Bertacchini, "A reconfigurable differential CMOS RF energy scavenger with 60% peak efficiency and -21 dBm sensitivity," *Microwave Wireless Components Letter, IEEE*, vol. 23, no. 3, pp. 155-157, Feb 2013.

[7] K. H. Choi; J. M. Park; J. K. Kim; T. S. Jung; K. D. Suh, "Floating-well charge pump circuits for sub-2.0 V single power supply flash memories," *VLSI circuits, 1997. Digest of Technical Papers, Symposium on*, pp. 61-62, June 1997.

[8] T. Umeda; H. Yoshida; S. Sekine; Y. Fujita; T. Suzuki; S. Otaka, "A 950 MHz rectifier circuit for sensor networks with 10-m distance," *Solid-State circuit, 2005. Digest of Technical Papers. ISSCC 2005. IEEE international*, vol. 1, no. 14, pp. 256-597, 2005.

[9] Z. Hamed; K. Moez; "Hybrid forward and backward threshold compensation RF-DC power converter for RF energy harvesting," *Journal on Emerging and Selected Topics in Circuits and Systems, IEEE*, vol. 4, no. 3, pp. 335-343, Sep 2014.

[10] H. M. Lee; M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," Transaction on Circuits and System. I, IEEE, vol. 58, no. 8, pp. 1749-1759, 2011.

[11] H. Nakamoto; D. Yamazaki; T. Yamamoto; H. Kurata; S. Yamada; K. Mukaida, T. Ninomiya; T. Ohkawa; S. Masui; K. Gotoh, "A passive UHF RF identification CMOS tag IC using Ferroelectric RAM in 0.35- µm technology", *Journal of Solid-State Circuits*, IEEE, vol. 42, no. 1, pp. 101–110, Jan 2007.

[12] Shailesh Singh Chouhan; Kari Halonen, "Internal Vth Cancellation scheme for RF to DC rectifiers used in RF Energy Harvesting", IEEE 2014.

[13] K. Kotani; T. Ito, "High efficiency CMOS rectifier circuit with Self-Vth Cancellation and power regulation functions for UHF RFIDs", *Solid-State Circuits, 2007.*

IEEE, Asian Conference, pp. 119–122. 238, Nov 2007.

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