A Wideband Bi-Directional Gain Amplifier with Asymmetric Cell using Cascade Gain Boosting in 65nm CMOS Process

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Abstract - **A bidirectional distributed gain amplifier (BDGA) with asymmetric cell combined with a cascade gain boosting structure is presented in this paper. Conventional DA designs generally have the gain limitation because of the additive gain mechanism, whereas the proposed structure can benefit significantly from the multiplicative gain mechanism due to the cascade of two BDGAs. Moreover, the unit gain cells are intentionally designed to be asymmetrical with the common source (CS) configuration at output stages to improve the output power of the circuit. The proposed circuit architecture is fabricated in a standard 65 nm CMOS. The measurement results show the gain of 10.5 dB, and the 3-dB bandwidth from 5.8 - 17.6 GHz. The measured output P_{1dB} is 6.8 dBm along with 9.3 dBm of the saturated output power at 10 GHz. The circuit draws a current of 75 mA from a 1.2 V supply and occupies 1.1 x 0.6 mm^2 of chip area.**

***Keywords*— Asymmetric cell, Bidirectional distributed CMOS, Gain amplifier, Gain boosting stage.**

I. INTRODUCTION

With the rapid progress of CMOS technology, which has been applied variously not only in defense industry but also commercial sectors such as automotive radar and high-speed communication, the active phased array technology has reached its maturity phase [1,2]. The transmit/receive module (TRM) plays the most critical role and has a significant impact on the entire cost and weight of active phased array systems. As a result, constant efforts have been putting into the research of new topologies for T/R module to reduce its cost, weight, power consumption, die area and simultaneously to increase its robustness and function [3]. Because the design of an active phased array front-end system requires thousands or even ten thousand of building elements, cutting down the cost per single TRM gives a substantial contribution to cost reduction of the phased array system especially in many low-cost applications [4]. Moreover, advances in digital signal processing have enabled digital beam forming mechanism in phased array system to integrate with amplitude and phase setting section. Digitally controlled phase shifter and attenuator consist of many CMOS switches which result in relatively high insertion losses due to the conductive silicon substrate. To recover the signal level from the losses of the aforementioned functional circuits, a broadband gain amplifier has to be included in the signal path of each T/R module. Since passive phase shifter and attenuator can operate in both transmit and receive directions, it is required that the gain amplifier should also be bi-directional to make the module more compact. The typical structure of a bi-directional amplifier is composed of two SPDT switches selecting signal paths between two separate amplifiers [5]. Even though this configuration can be optimized independently to achieve high output power transmission and low noise figure for receive paths, it shows poor high-frequency performance due to the loss of MOS switches and takes up large chip area because of separate amplifiers. As an attempt to remove T/R switches, a topology utilizing controllable impedance matching networks has been proposed [6]. This approach could separate the power amplifier and low-noise amplifier by setting different matching conditions directly via biasing. However, two separate amplifiers are still needed, and operable bandwidth is limited due to the impedance matching. Another way to remedy its shortcomings was by configuring common gate, which makes possible to select the amplification direction [7]. However, lossy MOS switches and low output power are significant drawbacks of this configuration. To resolve this weakness as mentioned earlier, taking the distributed amplifier's characteristic, which is well-known with its wideband, was proposed. The conventionally distributed amplifiers have been adapted to provide bi-directional operation by adding a parallel amplification branch for a "reverse direction mode." It can be a satisfactory solution for low-cost wideband applications [8, 9]. However, additive gain mechanism sets limitation upon the gain of the bidirectional distributed amplifier and also output power is not high enough.

This paper presents a new bidirectional distributed gain amplifier inherited broadband characteristic from the conventional distributed amplifier, high gain from the

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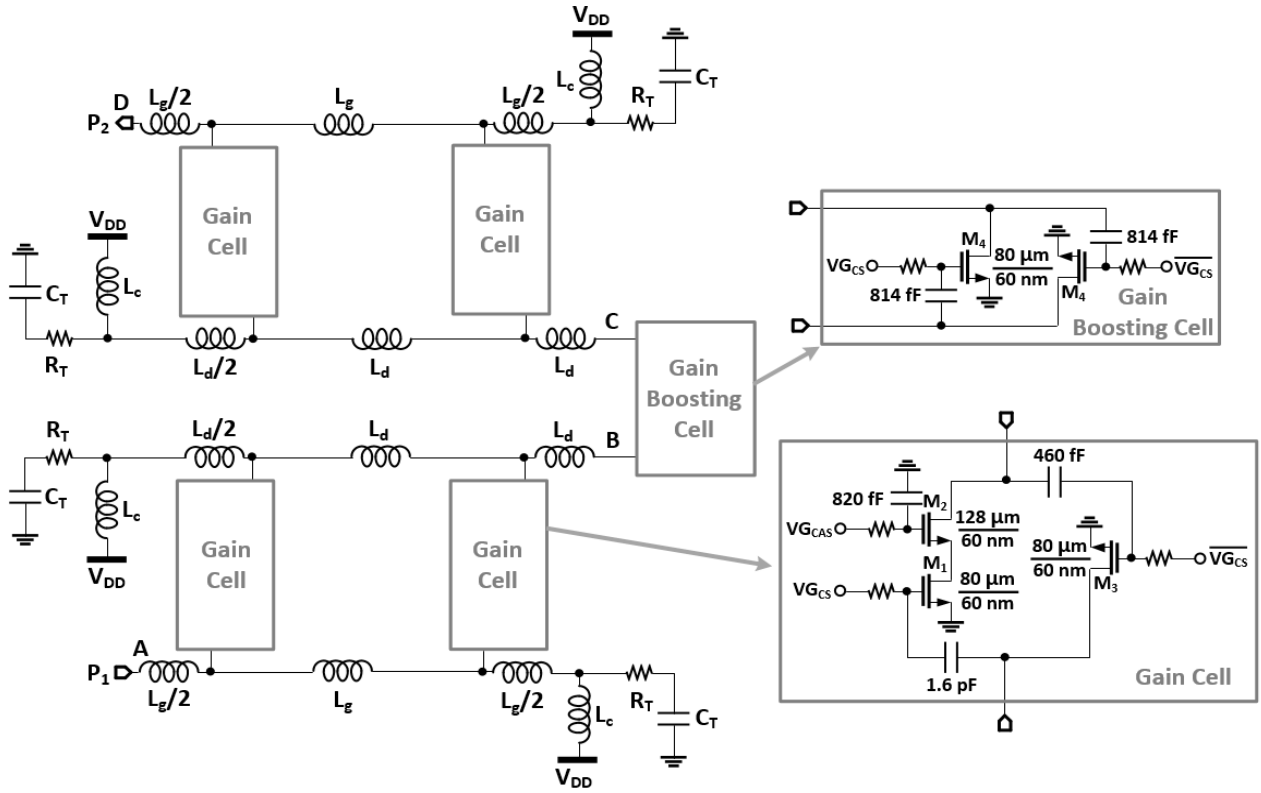

Fig. 1. The circuit schematic of new BDGA with gain and output power enhancement.

multiplicative mechanism, and high output power from the asymmetric gain cell configuration.

II. DESIGN OF BDGA

In general, with the assumption that the transmission lines are lossless, the voltage gain (G) of the conventional distributed amplifier can be expressed as:

$$\mathrm{G} = G_0\mathrm{N} = \frac{g_0 Z_0 N}{2} \tag{1}$$

where N is the number of the distributed stages, g_m represents the transconductance of a single stage, and G_0 is the gain of a single stage. The characteristic impedance Z_0 is typically 50 Ω. It is noteworthy that the factor of ½ implies that half of the output signal travels along the opposite direction towards the drain termination. As observed from the estimated gain equation, the conventional distributed amplifier shows the additive gain mechanism N × G_0 contrasting with the gain of a cascade of N amplifier stages which increase as G_0N. This fundamental characteristic of the conventional structure of distributed amplifier leads to the gain limitation, which is typically less than 10 dB for the reported designs.

Conventional BDGA shows that the limitation on the gain is from the additive gain mechanism as well as the loss of artificial transmission lines. To overcome this bottleneck, we cascaded two separate BDGAs with a common source (CS) stage. As demonstrated in Fig. 1, the circuit is composed of two 2-stage BDGAs and a CS stage for the gain-boosting in the middle. With the basic concept similarly to conventional BDGA, on-chip inductors and parasitic capacitances of transistors form the input and output artificial transmission lines which make the circuit broadband operation. Because of the cascade connection between each BDGA, the circuit takes advantage of the multiplicative gain mechanism. The voltage gain of cascade BDGA can be approximated by (2)

$$\begin{aligned} A_v &= A_{v1} \times A_{v2} \times A_{v3} \\ &= 2\left(g_{m1}\frac{Z_0}{2}\right) \times (g_{m2}Z_0) \times 2(g_{m3}\frac{Z_0}{2}) \end{aligned} \tag{2}$$

The number of gain cells in the first and third stages is chosen equal to two considering total chip area which is comparable with existing conventional BDGAs. If the building elements of all three cascaded stages are made the same, even though the gain can be significantly improved, the circuit introduces degradation in the output power. Hence, the first stage employs a cascode transistor pair configuration which is better for higher gain while second and third stages are made up by a single transistor in CS configuration demonstrating improvement on output power. The asymmetry of the unit gain cell does not affect the bidirectional function of the circuit. As can be seen in Fig. 1, the forward and backward paths are entirely identical. The detailed circuit schematics and device parameters of the gain cell and gain boosting stage are shown in Fig. 1.

The gain cell consists of cascode transistor pair (M_1 and M_2) in the forward direction and CS structure for reverse direction in connection with gate and drain inductors (L_G and L_D), 50 Ω termination resistors, and RF chokes inductors (L_C). Cascode configuration provides better gain-bandwidth and simpler biasing. The mechanism to control the operation mode of the amplifier is set by changing the bias voltages applied to gate terminals. For instance, in the forward mode operation, transistor M_1 and M_2 are ON in saturation region, and the transistor M_3 is OFF. The shunt capacitances at the input are comprised of the gate capacitance of M_1 in saturation and drain capacitance of M_3 in off, which along with gate inductances $L_D/2$ form the artificial transmission line whose characteristic impedance Z_0 is approximately expressed as:

$$Z_0 = \sqrt{L_G/C_G} = \sqrt{L_D/C_D} \quad (3)$$

By appropriately choosing MOSFET device sizes and inductor values, we can achieve Z_0=50 Ω of the artificial transmission-line. As a result, the circuit demonstrates wideband frequency response with better input and output return loss. To supply for the circuit in both operating modes, two V_{DD}'s are supplied at two ends of the amplifier. The capacitor at the gate of input transistor isolates its gate bias voltage from V_{DD}. All bias voltages are provided through 24 kΩ resistors as shown in the figure. All the parasitics and coupling of the passive elements were considered in design by performing 3D EM simulation with HFSS as shown in Fig. 2.

Fig.3 demonstrates the improvement of output P_{1dB} with asymmetric cell structure in which CS configuration is employed at the output stage in comparison with the symmetric one using symmetric cascode structure. Two different structures were investigated with post-layout simulation at the same DC bias current. The output P_{1dB} of the proposed cell structure is significantly better than that with the symmetric structure. Since the signal after the gain boosting cell is quite large, the use of the cascode structure at the output stage can degrade the gain and the output power. This is mainly because the amplifier at the output stage is saturated. Therefore, it is shown that the output P_{1dB} of the proposed asymmetric structure is much better than the symmetric structure.

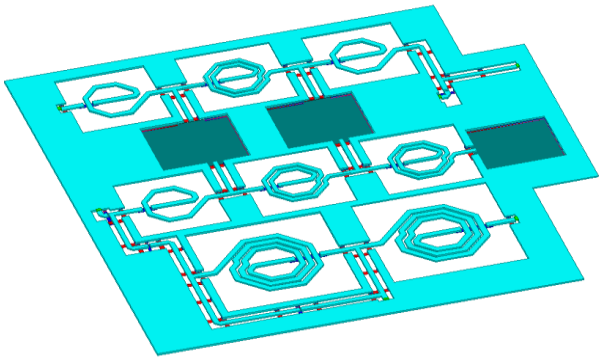

Fig. 2. Passive structure of BDGA simulated in HFSS.

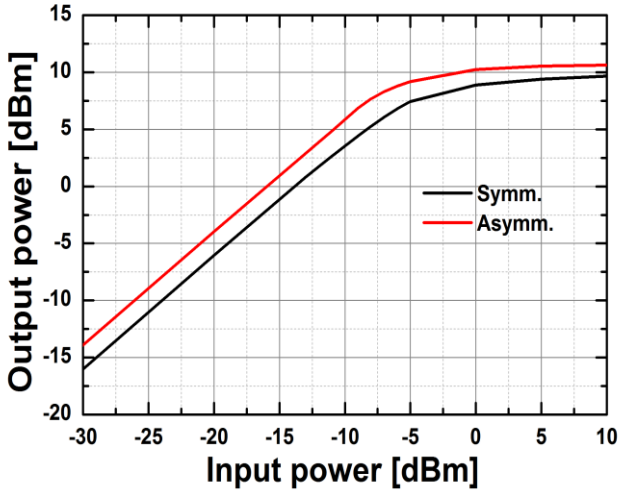

Fig. 3. The comparison between output powers of 2 different configurations.

Fig. 4 shows the voltage waveforms at nodes A, B, C, and D marked in Fig. 1, respectively. The dependence of circuit performance in temperature is shown in Fig. 5. As can be seen in Fig. 6, the proposed BDGA shows the group delay of lower than 150 ps from 4 – 24 GHz, which depends slightly on temperature. Regarding noise characteristic of the circuit, Fig. 7 presents the simulated results when varying the temperature.

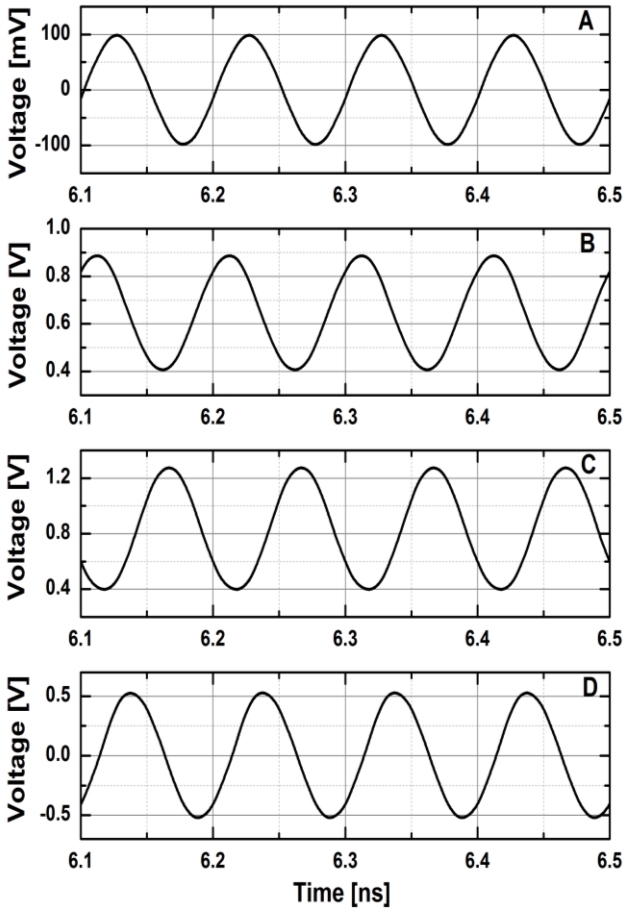

Fig. 4. The voltage waveforms at nodes A, B, C, and D marked in Fig. 1, respectively

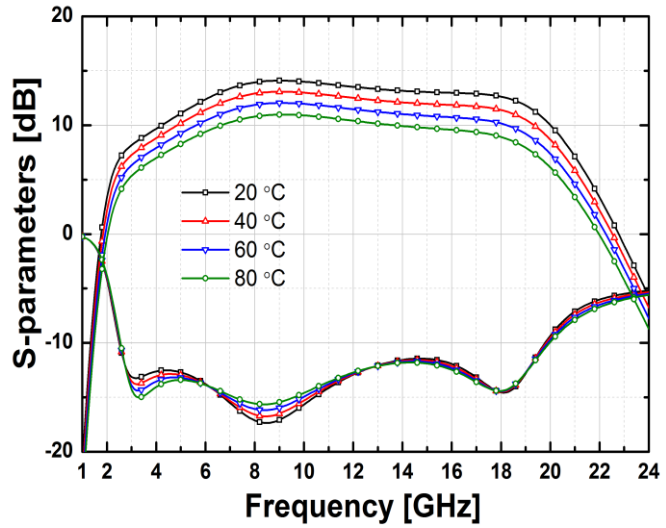

Fig. 5. Simulated S-parameters of the proposed BDGA depends on temperature.

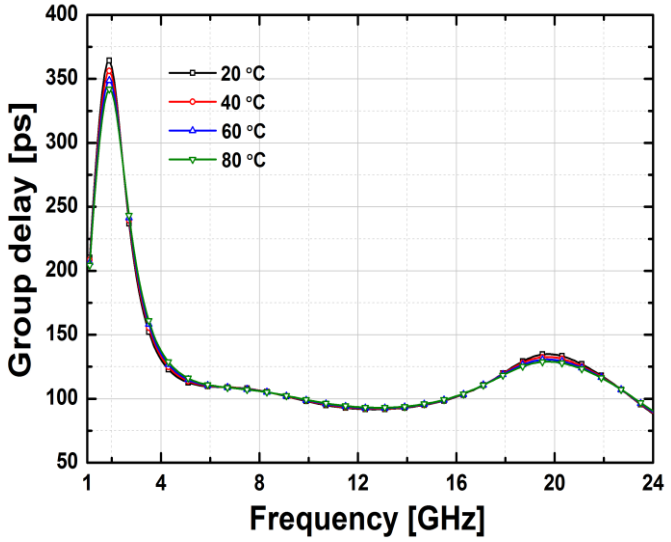

Fig. 6. Simulated group delay of the proposed BDGA

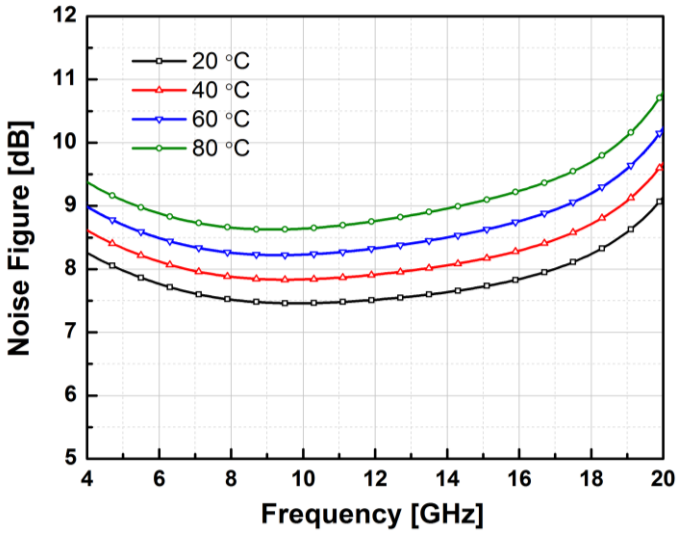

Fig. 7. Simulated noise figure of the proposed BDGA varying with temperature.

III. MEASUREMENT RESULTS

Fig. 8 shows the microphotograph of the implemented bi-directional distributed amplifier in Samsung 65nm CMOS technology. The implemented circuit occupies a die area of 1.1 x 0.6 mm^2 without pads. The setup for S-parameter measurement is sketched in Fig. 9. S-parameters are measured on-chip by Keysight PNA Network Analyzer with SOLT calibration. The measured results are correctly matched with the simulation as it is shown in Fig. 10. The transmission gain (S_{21}) of the fabricated BDGA is about 10.5 dB at 10 GHz, and input/output return losses are around 10 dB at 6 – 18 GHz. The isolation between the forward and reverse directions is better than 50 dB. Bi-directional performance of the implemented BDGA. As depicted in Fig. 10, the similarity between the forward and reverse directions is visualized in a graph. The measured output P_{1dB} is 6.8 dB m, and the saturated output power of the implemented BDGA is 9.3 dBm at 10 GHz as presented in Fig12.

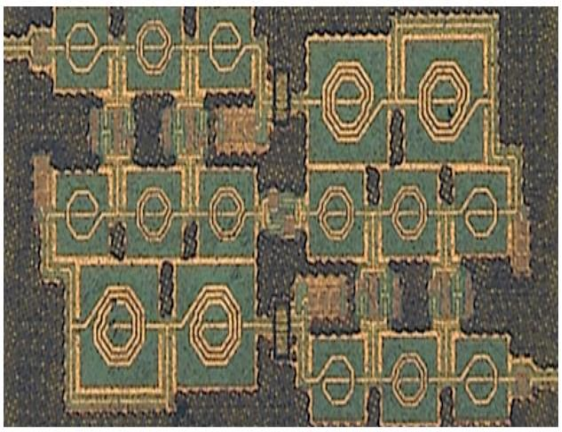

Fig. 8. The microphotograph of the proposed bi-directional distributed amplifier.

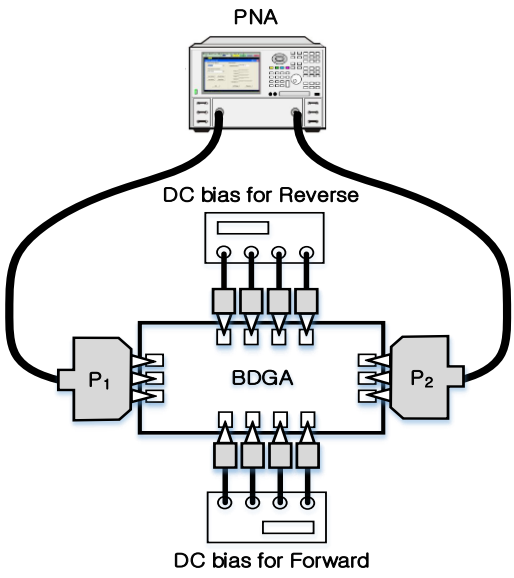

Fig. 9. Setup for S-parameter measurement of the fabricated BDGA.

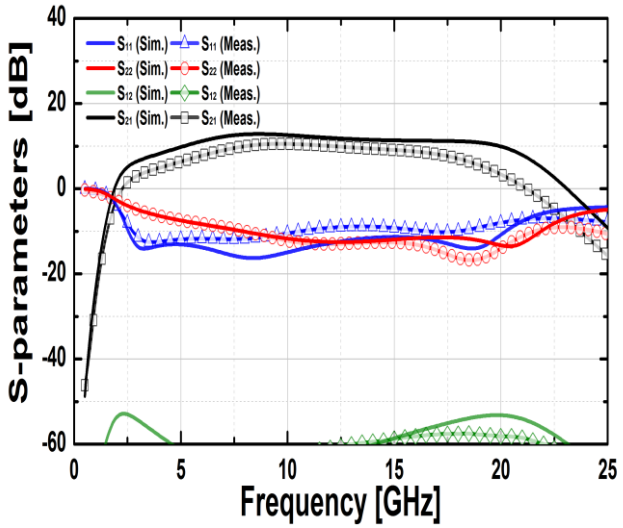

Fig. 10. The measured and simulated S-parameters of the BDGA

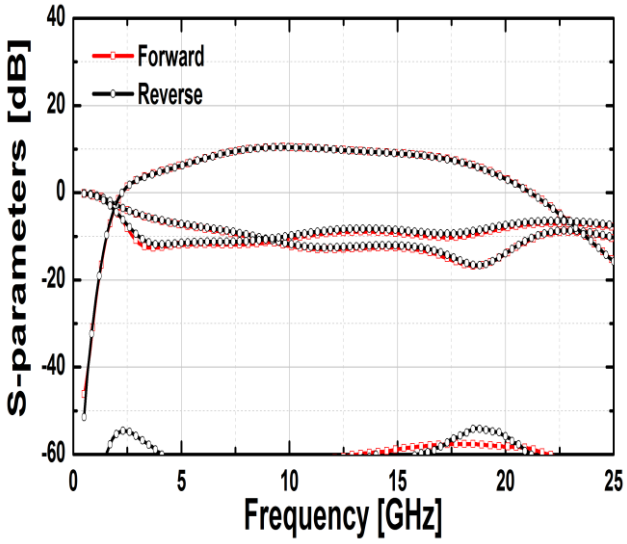

Fig. 11. The measured S-parameters of the BDGA in two directions.

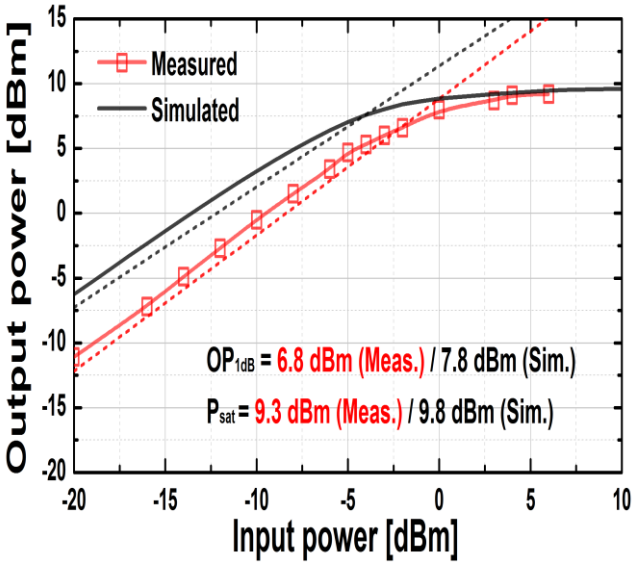

Fig. 12. The measured and simulated output power of the BDGA at 10 GHz.

IV. CONCLUSIONS

A bi-directional distributed gain amplifier with relatively high gain and high output P_{1dB} is presented. The proposed amplifier utilizes a cascaded stage in the middle of the distributed amplifier to boost gain and consists of the asymmetric bi-directional gain cells to improve the output P_{1dB}. The fabricated BDGA achieves 11.8 GHz of the 3-dB gain-bandwidth (5.8 - 17.6 GHz), 6.8 dBm of output P_{1dB} and 11 dB of the saturated output power whereas drawing 75 mA from a 1.2 V supply.

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