Design of a 10-bit SAR A/D converter with 2-bit/step and threshold configuring comparator

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***Abstract* - In this paper, we designed an A/D converter that can be applied to a system that enables interface between human body and device such as touchpad. As devices become more sophisticated, higher operating speeds are required. Portable devices have been developed to minimize power consumption and miniaturize devices. The upper 5 bits are determined by digital code using a reference voltage variable comparator. The reference voltage variable comparator changes the offset by connecting the current path to the input pair, and the reference voltage is sequentially shifted according to the digital code of the upper 5 bits. The lower 5 bits change the reference voltage by the switching of the capacitor D/A converter to determine the digital code. This technique reduces the capacitance of the capacitor D/A converter, reduces dynamic power consumption, and reduces chip area. The clock double circuit reduces the period of the external clock by 2 times and increases the operation speed by 2 bits per step. The designed 10 - bit SAR A/D converter was fabricated with Magna chip 0.18μm CMOS 1Poly 6Metal process. Simulation results showed 56 power consumption and 9.5 bit ENOB at maximum sampling frequency of 10MHz for 1.8V supply voltage and 1 kHz sinusoidal input. The proposed SAR A/D converter with 7.73fJ/step FoM is expected to be applied to low power systems.**

***Keywords*—A/D converter, Clock double, Offset voltage, Reference voltage variable comparator**

I. INTRODUCTION

Currently, the importance of the low-power design is greater than any time. Since there is no circuit that consumes static power inside the circuit, successive approximation register (SAR) A/D converter is a critical factor.

The largest power of the SAR A/D converter is the switching power of the capacitor D/A converter (C-DAC). Decreasing the capacitor capacity of the D/A converter reduces power consumption. However, SAR A/D converters require multiple clocks instead of one clock to determine the digital code [1-2]. This has disadvantages in high-speed design. In order to overcome these drawbacks, a multi-bit SAR A/D converter that determines two or more bits in one step is being studied [4-7]. In the case of multi-bit (N-bit) and two or more C-DACs are used, which takes additional chip area and increases switching power. The operating speed increases but the additional power consumption is needed. There are ways that the capacitor to consume less power. Circuits that do not use a C-DAC by changing the reference voltage of a comparator using a threshold configuring comparator (TCC) have been used [3]. This reduces the power consumption of the C-DAC and occupies smaller chip area. However, there is a limitation in high-resolution design due to the mismatch of process and errors in TCC. In the proposed circuit, the TCC is applied to the upper 5 bits and the lower 5 bits designed to be compared through the switching of the C-DAC like the existing SAR A/D converter. When using the TCC to determine the upper 5 bits, it is possible to reduce the upper capacitor which occupies the most part in the C-DAC, which enables to design low-power system with reduced chip area. The TCC is designed to determine the lower bits through the switching of the C-DAC when comparing low-order bits where a reference error occurs and a detailed comparison is required when process mismatch occurs. The 10 bit SAR A/D converter using the reference voltage variable comparator (TCC) proposed in this study is applied to the upper 5 bits of the comparator that sets the reference voltage by changing the size of the two input transistors, and a C-DAC for the lower 5 bits to reduce chip area and switching power consumption. Then two bits per step using a clock double circuit results are compared with the proposed circuit.

II. THE PROPOSED ARCHITECTURE

The SAR A/D converter with the reference voltage-variable comparator changes the offset of the comparator without using the capacitor D/A converter in order to remove the switching power of the capacitor D/A converter which demands the most part of the total power. An A/D converter for comparison was used. Figure 1 (a) shows the structure of a SAR A/D converter using a reference voltage-variable comparator. The SAR A/D converter with a reference voltage-variable comparator consists of a reference voltage-variable comparator, sample-and-hold, and SAR logic and a reference-voltage-variable comparator control logic. Unlike the general structure shown in Figure. 1 (b), since there is no capacitor D/A converter, there is no switching power of the capacitor. As a result, the power consumption can be reduced. When a signal is input through the sample and hold,

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Manuscript Received Sep. 30, 2018, Revised Dec. 20, 2018, Accepted Dec. 31, 2018

the MSB is determined by changing the offset of the comparator by / 2, and the offset is adjusted by ± 4 according to the result of the MSB to determine the digital code. In this way, the offset is changed by ± / to convert to LSB

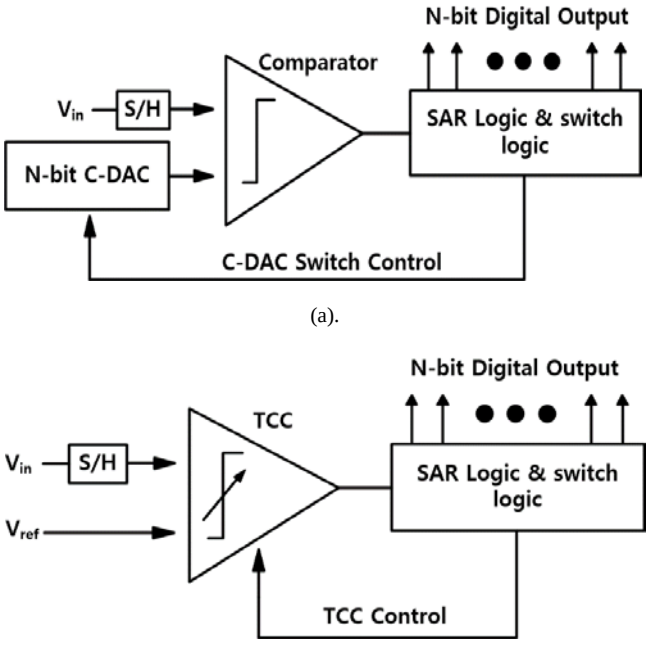


Fig. 1. The structure of SAR A/D Converter

(a) Conventional (b) Structure with TTC

Figure 2 is a block diagram of the 10-bit SAR A/D converter using the proposed reference voltage variable comparator and 2-bit per step technique. The entire circuit consists of a reference voltage variable comparator used to compare the upper bits and a reference voltage variable comparator control logic to adjust the offset of the comparator, a capacitor D/A converter for the lower 5 bits, a clock double circuit to supply the clock signal of the circuit, a reset generation circuit, a switch control logic circuit, an SAR logic circuit, and an output register. The reference voltage variable comparator changes the reference voltage by changing the offset in the upper bit and does not change the offset in the lower bit, thereby becoming a general comparator capacitors for lower bits. The D/A converters use scaled capacitors to reduce the capacitance of the capacitors, reducing chip area and power consumption.

A reference voltage variable comparator is often used to compensate for the offset of the comparator due to process mismatch. A common reference voltage-variable comparator is either using an asymmetrical capacitor load or using an asymmetrical current path. Figure 3 shows a reference voltage-variable comparator using an asymmetrical current path. The comparator consists of two stages, the first stage connecting the same proportion of the current path across the input transistor to produce the offset of the comparator. The second stage is the latch stage, which detects and amplifies the pull-down time of the nodes X and Y of the first stage to determine the digital output. When the CLK signal is '0', M4 and M5 are turned on, and M3 is turned off, so that nodes X and Y are pulled up. When nodes X and Y are present, the latch stage outputs are all pulled down to zero. This is called reset mode. When the CLK signal is '1', the comparator mode is selected and the two input values are compared. Conversely, M4 and M5 are off, and M3 is on and nodes X and Y are pulled down. Since the input values of M1 and M2 are different, the resistance value is different Therefore, the voltage pull-down time of the nodes X and Y becomes different from each other. This pull-down time difference is amplified through the latches to compare the two input values.

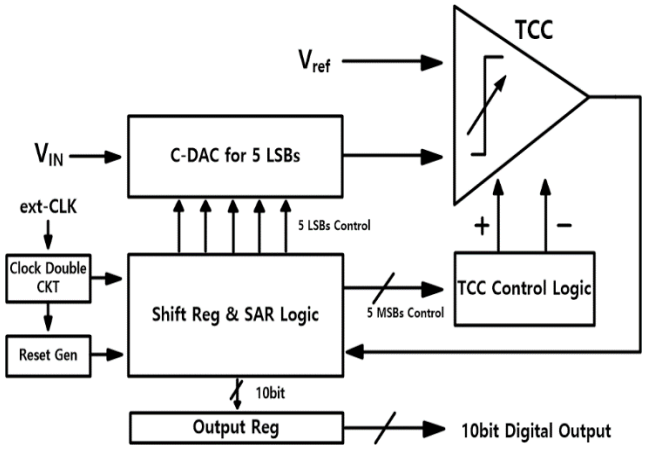


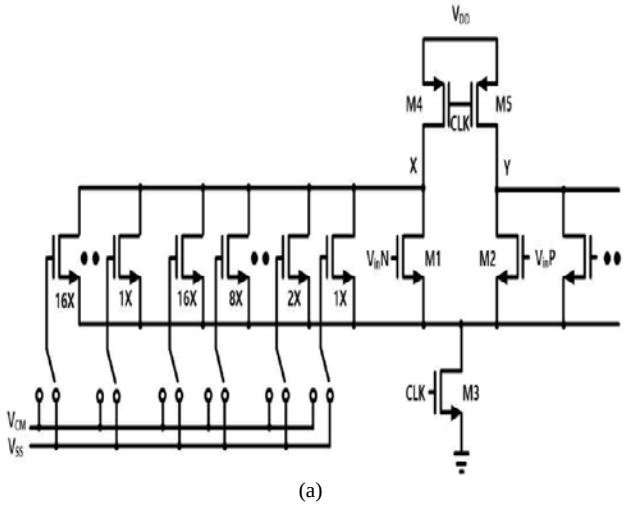
Fig. 2. A 10-bit SAR A/D converter with 2-bit/Step and threshold configuring comparator

The amount of charge stored in nodes X, Y of the input pair and the time to pull down is (1).

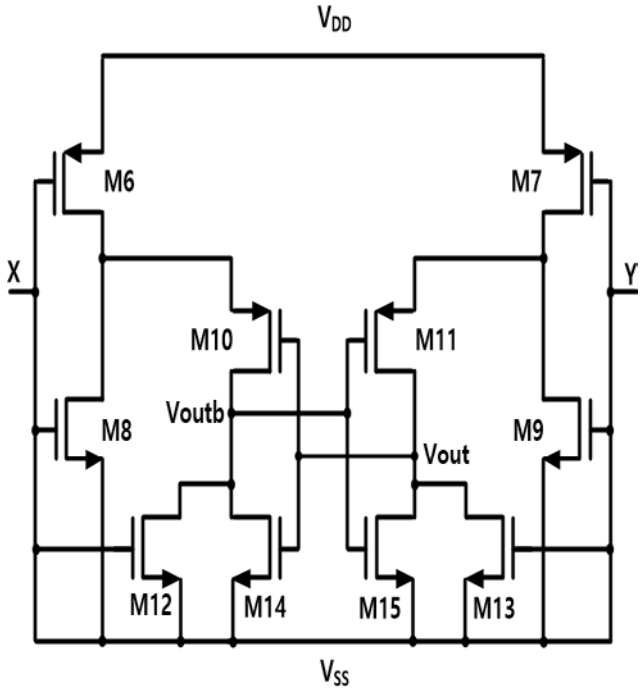
$$t_{latch}=\frac{C*V_{latch}}{I_d} \quad (1)$$

If the voltage that is pulled down is obtained over ti me is (2).

$$V(t) = V_{OC} + (V(0) - V_{OC})e^{-t/RC} \quad (2)$$



(a)



(b)

Fig. 3. The schematic of threshold configuring comparator
(a) Threshold configuring stage (b) Latch stage

Table1 shows the offset voltage change of the comparator according to the upper 5 bits. The change of the offset voltage of the comparator changes from $^{1}/_{32}\,V_{ref}$ to $^{15}/_{32}\ V_{ref}$.

TABLE I.
Offset variation with 5MSB

5MSB (B9~B5)	Offset variation	5MSB (B9~B5)	Offset variation	5MSB (B9~B5)	Offset variation	5MSB (B9~B5)	Offset variation
B9='1' 11000	$-V_{ref}/4$	B8='1' 11100	$3V_{ref}/8$	B7='1' 11110	$-7V_{ref}/16$	B6='1' 11111	$-15V_{ref}/32$
						B6='0' 11101	$-13V_{ref}/32$
				B7='0' 11010	$-5V_{ref}/16$	B6='1' 11101	$-11V_{ref}/32$
						B6='1' 11001	$-9V_{ref}/32$
		B8='0' 10100	$-V_{ref}/8$	B7='1' 10110	$-3V_{ref}/16$	B6='1' 10111	$-7V_{ref}/32$
						B6='0' 10101	$-5V_{ref}/32$
				B7='0' 10010	$V_{ref}/16$	B6='1' 10011	$-3V_{ref}/32$
						B6='0' 10001	$-V_{ref}/32$
B9='0' 01000	$+V_{ref}/4$	B8='1' 01100	$+V_{ref}/8$	B7='1' 01110	$+V_{ref}/16$	B6='1' 01111	$+V_{ref}/32$
						B6='0' 01101	$+3V_{ref}/32$
				B7='0' 01010	$+3V_{ref}/16$	B6='1' 01011	$+5V_{ref}/32$
						B6='0' 01001	$+7V_{ref}/32$
				B7='1' 00110	$+5V_{ref}/16$	B6='1' 00111	$+9V_{ref}/32$
						B6='0' 00101	$+11V_{ref}/32$
		B8='0' 00100	$+3V_{ref}/8$	B7='0' 00010	$+7V_{ref}/16$	B6='1' 00011	$+13V_{ref}/32$
						B6='0' 00001	$+15V_{ref}/32$

The proposed SAR A/D converter reduces the interna l clock period to decrease the number of comparators in the conventional 2 bit SAR A/D converter per step, and determines 2 bits per step by comparing twice in one cycle. Figure 4 (a) shows the waveform of the ex ternal clock and internal clock. And an exclusive OR circuit with a delay cell for delaying the input clock. Compares the input clock, X, which is the delay of th e input clock, and outputs '1' if the value is different, and '0' if the value is the same. Figure 4 (b) shows the schematic of the clock double circuit.

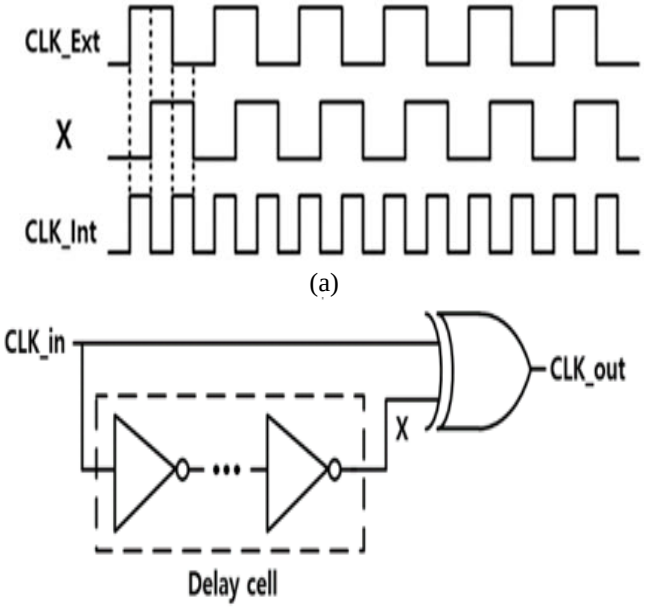


Fig. 4. The clock double circuit
(a) External clock and internal clock (b) Schematic

Figure 5 shows an SAR logic circuit constructed using D flip-flop columns. The SAR logic circuit is the core logic circuit for carrying out the binary approximation process of the SAR A/D converter. The SAR logic consists of a shift register and an output stage. The shift register is a circuit for moving the reset waveform to the flip-flop side according to the clock signal, and sets the output signal of each flip-flop at the output end according to the shifted signal to advance the binary approximation process. In the detailed operation of the circuit, the reset waveform is connected to the set of the first flip-flop of the shift register, and the output becomes '1', the other flip-flop set is connected to the ground and the output of the remaining flip- The output of all shift registers starts with '1000000000'. When the clock is applied, the output of the first flip-flop is shifted to the input of the second flip-flop and the output becomes '0100000000'. As a result, '1' of the reset waveform is shifted by one time. The output of the shift register is connected to the set of the output stage, respectively, to set the output stage. The first output of the shift register, '1000000000', is the output of the output stage. This value becomes the input of the switch of the capacitor D/A converter and subtracts / 2 from the sampled input signal to the output of the capacitor D/A converter. V_{ref}/ 2 and the input signal are compared in the comparator, and the output of the comparator is input to D of all the flip-flops of the output stage. In the next step, when

the shift register becomes '0100000000', the output of the second flip-flop of the output stage is triggered to '1' and this signal is applied to the clock of the first flip-flop and triggered so that the MSB is stored in x of 'x100000000' . In the next step, the output digital code is stored in this manner.

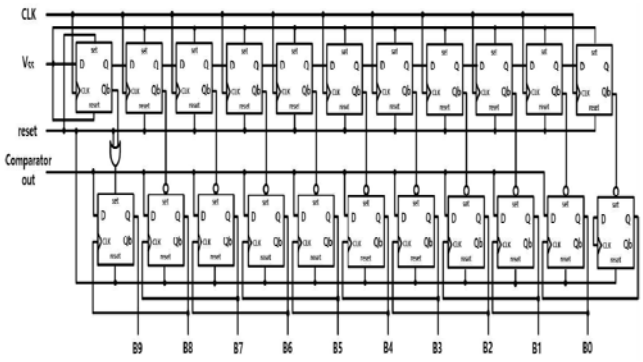


Fig. 5. SAR Logic Circuit

III. RESULTS AND DISCUSSION

The proposed A/D converter is designed using Magna chip 0.35μm CMOS 2Poly 4Metal process. Figure 6 is a layout photo of the designed SAR A/D converter, with an area of 700 x 750. The line simulation has a supply voltage of 1.8V, a reference voltage of 1.2V, and the range of the analog input signal is 1.2V. The restored output signal of the SAR A/D converter designed for a sinusoidal input signal at a sampling frequency of 10 MS/s and a frequency of 1.5 kHz is shown in Figure. 7, and the spectral results are shown in Figure 8. Post simulation result is extracted with only capacitor (The reconstructed signal uses a rectangle window with 16384 samplings. The SNDR is 60.12dB, the SFDR is 63.68dB, and the effective number of bits is 9.7 bits. As a result of the simulation, the power consumption was measured as 53, and the performance evaluation index FoM was 6.37 fJ / step. The performance of the SAR A/D converter measured by the experiment is summarized in Table 1.

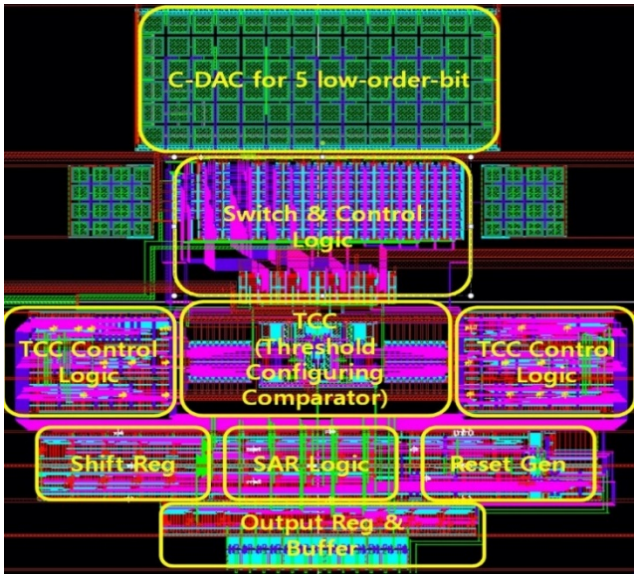


Fig. 6. Layout of propose SAR A/D converter

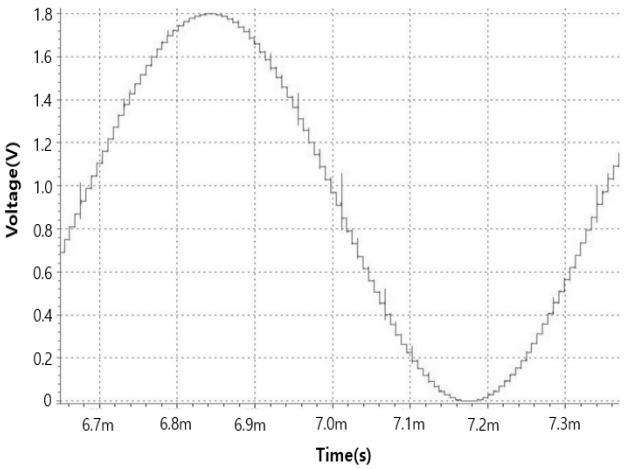
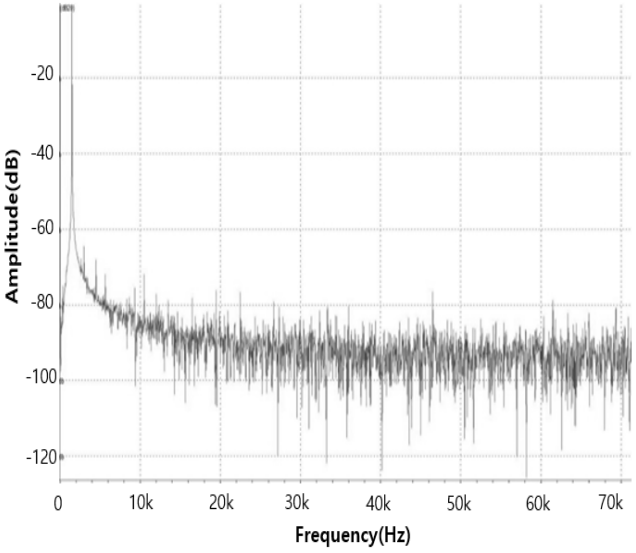
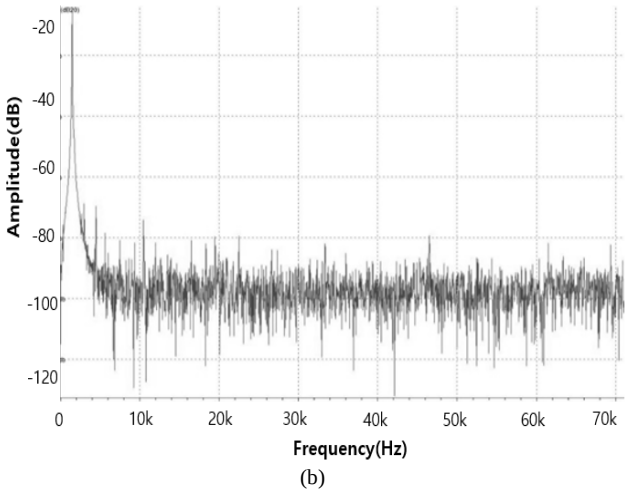


Fig. 7. Restoration waveform of input signal



(a)



(b)

Fig. 8. FFT simulation result
(a) Pre simulation (b) Post simulation

The parasitic elements were extracted and simulated using hspice. A sine wave input signal with a sampling frequency of 10MS / s and a frequency of 1.5 kHz is applied. The restored signal was sampled 16,384 times, using the

rectangle window. The measured SNDR is 58.02.dB, the SFDR is 60.95dB, and the effective bit number is 9.5 bits. Figures 9 and 10 show the changes of SNDR and ENOB for the input signal. In Figures 11 and 12, INL and DNL were measured as 1 LSB and 0.5 LSB, respectively. The power consumption was measured as 56 and the performance evaluation index FoM was measured as 7.73 fJ / step.

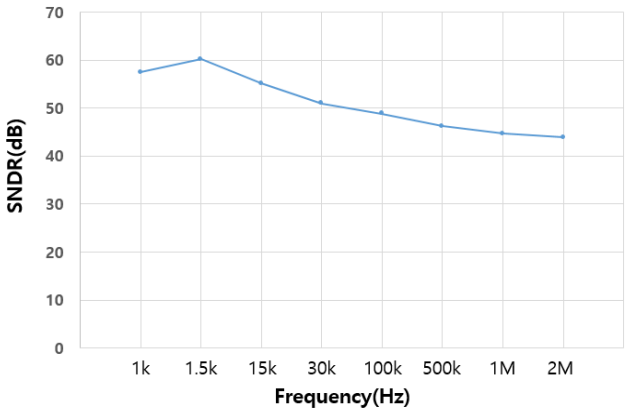


Fig. 9. Variation of SNDR versus input frequency

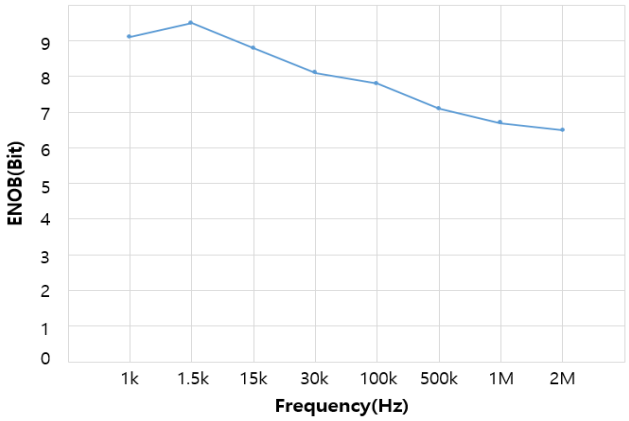


Fig. 10. Variation of ENOB versus input frequency

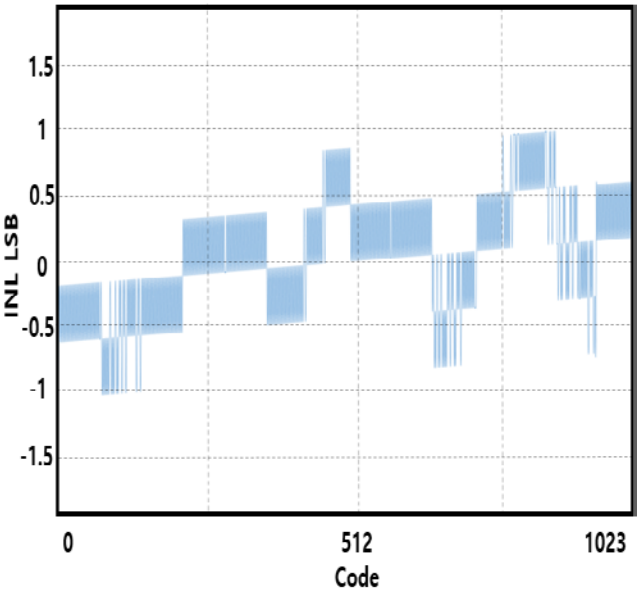


Fig. 11. Post-simulation result of INL

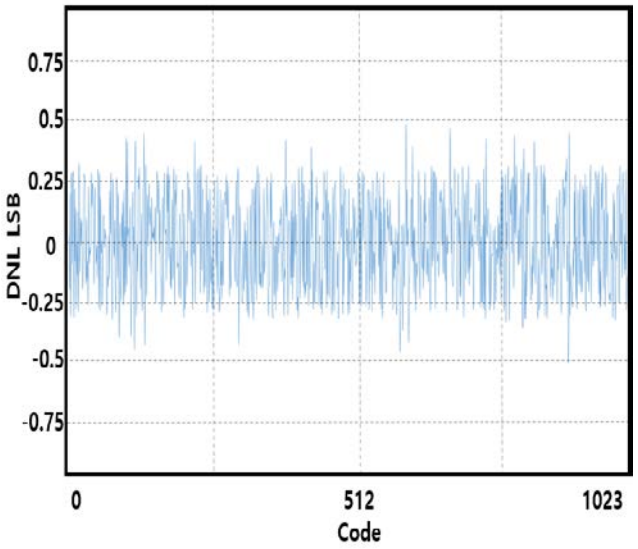


Fig. 12. Post-simulation result of INL

TABLE II.

Comparison of performance

Parameter	2015[1]	2009[2]	2015[4]	2012[7]	2014[14]	This work (post-simulation)
Architecture	2bit/step	2bit/step	2bit/step	2bit/step	2bit/step	2bit/step
CMOS Process	40 nm	0.13 μm	45 nm	65 nm	0.18 μm	0.18 μm
Resolution(bit)	8	6	7	8	10	10
Supply voltage(V)	0.8	1.2	1.25	1.2 / 1	0.6	1.8
Input range(V)	-	1.2	-	-	1.2	1.2
Speed	40.96 MS/s	1.25 GS/s	1 GS/s	400 / 250 MS/s	100 KS/s	10 MS/s
SNDR(dB)	45.8	-	40.8	44.5 / 46.7	-	58.02
ENOB(bit)	7.32	5.5	-	-	9.2	9.5
Power consumption	107 μW	32 mW	7.2 mW	4 / 1.8 mW	390 nW	56 μW
FoM	16 fJ/step	-	80 fJ/step	73 / 42 fJ/step	6.7 fJ/step	7.73 fJ/step

ACKNOWLEDGMENT

This work was supported by the IDEC

REFERENCES

[1] Kentaro Yoshioka, Akira Shikata, Ryota Sekimoto, Tadahiro Kuroda and Hiroki Ishikuro, “An 8 bit 0.3−0.8 V 0.2−40 MS/s 2-bit/Step SAR ADC With Successively Activated Threshold Configuring Comparators in 40 nm CMOS”, IEEE Transactions on VLSI Systems, vol. 23, no. 2, pp. 356-368, Feb. 2015.

[2] Zhiheng Cao, Shouli Yan and Yunchu Li, “A 32 mW 1.25 GS/s 6b 2b/Step SAR ADC in 0.13 um CMOS”, IEEE Journal of Solid-State Circuits, vol. 44, no. 3, pp. 862-873, Mar. 2009.

[3] Pierluigi Nuzzo, Claudio Nani, Costantino Armiento, Alberto Sangiovanni-Vincentelli, Jan Craninckx and Geert Van der Plas, “A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS”, IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, no. 1, pp. 80-92, Jan. 2012.

[4] Hyeok-Ki Hong, Wan Kim, Hyun-Wook Kang, Sun-Jae Park, Michael Choi, Ho-Jin Park and Seung-Tak Ryu, “A Decision-Error-Tolerant 45 nm CMOS 7b 1 GS/s Nonbinary 2b/Cycle SAR ADC”, IEEE Journal of Solid-State Circuits, vol. 50, no. 2, pp. 543-555, Feb. 2015.

[5] Hualing Wu, Qiao Meng and Hao Zhi, “A novel 10bit 90MS/s 2b/cycle SAR ADC”, 2013 International Conference on ATC, pp. 521-524, 16-18 Oct. 2013.

[6] Guoxian Dai, Chixiao Chen, Shunli Ma, Fan Ye and Junyan Ren, “A 400-MS/s 8-b 2-b/cycle SAR ADC with shared interpolator and alternative comparators”, 2014 IEEE ISCAS, pp. 2365-2368, 1-5 Jun. 2014.

[7] Hegong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui Paulo Martins and Franco Maloberti, “An 8-b 400-MS/s 2-b-Per-Cycle SAR ADC With Resistive DAC”, IEEE Journal of Solid-State Circuits, vol. 47, no. 11, pp. 2763-2772, Nov. 2012.

[8] Yan Zhu, Chi-Hang Chan, Seng-Pan U and Rui Paulo Martins, “An 11b 450 MS/s Three-Way Time-Interleaved Subranging Pipelined-SAR ADC in 65 nm CMOS”, IEEE Journal of Solid-State Circuits, vol. 51, no. 5, pp. 1223-1234, May. 2016.

[9] Frank van der Goes, Christopher M. Ward, Santosh Astgimath, Han Yan, Jeff Riley, Zeng Zeng, Jan Mulder, Sijia Wang and Klaas Bult, “A 1.5 mW 68 dB SNDR 80 Ms/s 2x Interleaved Pipelined SAR ADC in 28 nm CMOS”, IEEE Journal of Solid-State Circuits, vol. 49, no. 12, pp. 2835-2845, Dec. 2014.

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