Design of a CMOS Current-reuse LC VCO

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***Abstract* - This paper presents a cascode CMOS current-reuse voltage-controlled oscillator (LC VCO) for 24GHz automotive collision radar. This circuit is designed using 65nm CMOS technology. The VCO in modified current-reuse configuration where transistors are biased in subthreshold region to save power consumption. This scheme is utilized to simultaneously reduce the power consumption, and increase the transconductance and gain of the VCO circuit. The capacitive-feedback technique, including two series capacitors is also used to improve voltage swing of output ports under low power and low supply voltage conditions. This circuit also has fully-differential configuration to reduce RF noise and harmonic distortion. The proposed VCO showed phase noise of -123dBc/Hz at 1MHz offset, and power consumption of 321μW at power supply of 950mV with a FOM of -204 dBc/Hz. The die area occupied 0.35mm2.**

***Keywords*—Capacitive-feedback technique, Current-reuse structure, Voltage-controlled oscillator (VCO)**

I. INTRODUCTION

Nowadays, one of the serious global concerns is road traffic crashes. To enhance safety, automotive radar-based assistance systems are now installing on many transport and luxury passenger vehicles. The main frequency bands of radar applications are 24GHz as well as 77GHz. For the sake of detection other near vehicles in the medium-short range and wide beam, 24GHz is the mainstream [1-3].

ecently with the downscaling of CMOS technology, implementation of highly integrated low phase noise, low voltage and low power dissipation VCOs is one of the major challenges in the RF frontend modules. Among the diverse types of oscillators, LC VCO has been widely used thanks to its better phase noise at low supply voltage and its relaxed and reliable start-up mode. In the battery-driven systems, local oscillator (LO) still consumes a great portion of the current in the frontend; hence low phase noise and low power dissipation are two of crucial factors in designing procedure of VCO to reduce bit error rate (BER) and to increase the battery life-span.

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In this paper, a cascode current-reuse structure is utilized to simultaneously reduce the power consumption and increase the transconductance and gain of the VCO circuit. The capacitive-feedback technique, including two series capacitors is also used to improve voltage swing of output ports under low power and low supply voltage conditions.

II. CIRCUIT DESIGN

The design and implementation of single-chip transceivers have already been demonstrated in CMOS technologies for RF CMOS integrated circuits (*ICs*). For wireless communication circuits, voltage-controlled oscillators (*VCOs*) are key elements of the transceivers. Oscillator is an independent circuit, since some self-sustaining mechanism generates a periodic stable sinusoidal signal. VCO also can be used as a part of the frequency synthesizer to produce the local oscillator signal for both down-conversion and up-conversion mixers. Oscillation can be sustained by providing the system with an appropriate amount of positive feedback or negative resistance that can compensate any loss in the circuit as shown in Figure 1. Due to the better relative phase noise performance of inductance-capacitance, (*LC*) tank oscillators are preferred to ring oscillators for monolithic integration in CMOS technology. Beside the limitations in the applied semiconductor technology an ideal VCO should meet most of these specification such as low phase noise, low power, wide tuning range, high integration, small die area accuracy and low cost.

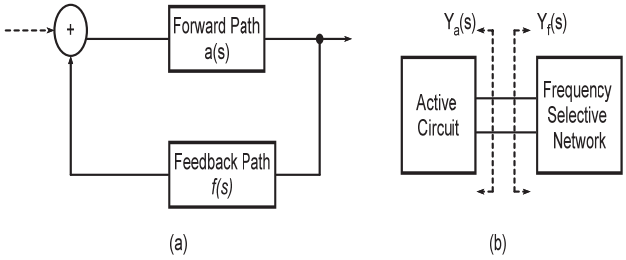


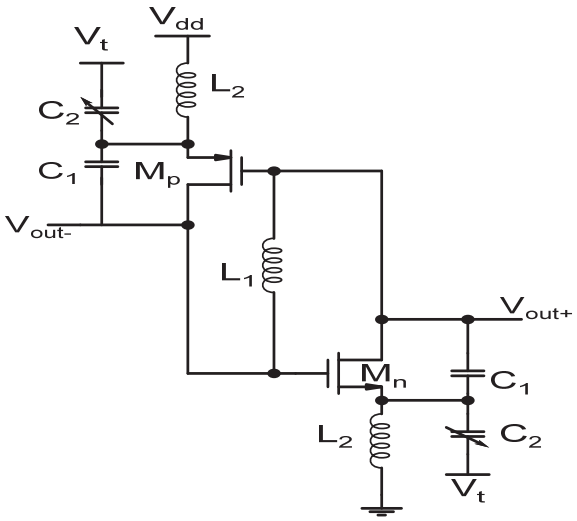
Fig. 1. (a) Feedback model, and (b) negative resistance model.

The ring oscillator is classified as a waveform oscillator and it displays advantages such as high integration in VLSI and wide tuning range, and small chip area. Usually, it generates lower frequencies than the LC tank ones, so this feature leads to reduce the complex pre-scaler requirements or frequency dividers that occupy large space and contribute

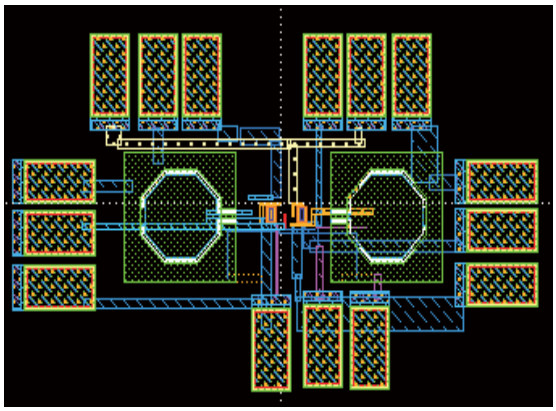
to their own noise. LC oscillators achieve lower phase noise in comparison with ring ones for a given power consumption. Thus, LC VCOs are often preferred for higher frequencies with low power and low phase noise. One obvious disadvantage of LC VCO is to use an/more inductor(s) and often variable capacitors to control the tuning voltage which occupy large area on the chip. Therefore, LC VCOs are not well-suited for VLSI implementation.

The phase noise characteristics of LC tank VCOs at low power supplies are superior to that of the ring oscillators, and as the technology is being further downscaled, this feature is becoming increasingly crucial. For the applied tuning and the resulting output frequency, the frequency tuning characteristics of the ring oscillator display a fairly linear behavior. However, at lower power supplies, as the phase noise becomes more dominant, the linearity suffers more and more.

Varactors, variable reactors, or voltage controlled capacitors based on MOS structure are widely used as tunable capacitors in LC VCOs, and their capacitance features define the output oscillator frequency.



(a) Circuit



(b) Layout

Fig. 2. The proposed current-reuse LC VCO schematic and chip microphotograph with capacitive-feedback technique.

Also, it is hard to predict the output of VCOs because large amplitude swings at the LC VCO output impact the effective capacitance of the varactor modulating the output frequency. When a varactor with abrupt capacitance characteristics is used in an LC VCO, and the oscillator amplitude swing is directly applied across it, the frequency curve shows strong dependence on the bias current (I_{bias}). Distortion is also introduced by the bias current and the oscillation sustaining active elements and it corrupts the output frequency curve by the up-conversion of various noise sources to the resonance frequency.

The other factors that severely reduce the capacitance tuning range are parasitic capacitances of tank inductor, the drain overlap capacitances, wiring and gate to source capacitances.

Fig. 2. The tail current-shaping transistor in conventional cross-coupled LC VCO [2] is replaced by inductor to reduce the power supply and eliminate the pertinent noise resulting in a high phase noise. The capacitive-feedback technique including C_1 and C_2 is utilized to enhance the output swing of LC VCO. The composition of on-chip inductors and capacitors in the capacitive-feedback technique causes the drain and source voltage of MOS transistors swing above the supply voltage (V_{dd}) and below the ground (zero). Since the varactors in the proposed current-reuse LC VCO are utilized in parallel with source terminals, a small change on their values leads to a large variation in the frequency. Furthermore, the proposed circuit shows a reasonable phase noise thanks to employing cascode current-reuse structure and elimination of current-shaping source. Further analysis of the proposed circuit is presented as follows.

Let's consider the equivalent small-signal of the half-circuit without negative resistance, L_1 and L_2 are the LC tank inductors with R_{P1} and R_{P2} losses, respectively. It's worthwhile to remark that the parasitic capacitances of the transistors which are smaller than the C_1 and C_2 are neglected. For the sake of simplicity in the calculation the losses of the inductors are assumed to be parallel with inductors as shown in Fig. 2.

The half-circuit equivalent small-signal without negative resistance of the proposed current-reuse LC VCO is illustrated in Fig. 3. Inductors L_1 and L_2 are the LC tank inductors with R_{P1} and R_{P2} losses, respectively. The parasitic capacitances of the transistors smaller than the C_1 and C_2 are neglected.

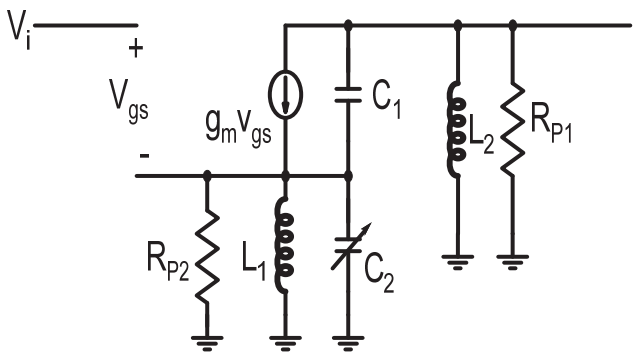


Fig. 3. Small signal half-circuit model of LC VCO.

The current-reuse topology provides a center-tab node A, shown in Fig. 3, where is placed between two inductors L_1. Since the n/pMOS transistors operate in the differential mode, the center-tab node functions as a virtual ground and hence it simplifies the DC self-biasing and high frequency analysis. For the sake of simplicity in the calculation the losses of the inductors are assumed to be parallel with inductors as shown in Eq. (1) and Eq. (2).

$$R_{P_1} = \frac{\omega^2 L_1^2}{R_{S_1}} \quad (1)$$

$$R_{P_2} = \frac{\omega^2 L_2^2}{R_{S_2}} \quad (2)$$

where R_{s1} and R_{s2} are the series resistors of L_1 and L_2, respectively.

After cumbersome calculation and proper arrangement of the loop gain unity (V_o/V_i) at ω_0 the result is as follows:

$$L_1L_2C_1C_2\omega_0^4 - \left[L_1C_1 + L_2(C_1 + C_2) - \frac{L_1L_2g_m}{R_{p2}}\right]\omega_0{}^2 + 1 = 0 \quad (3)$$

$$L_1L_2(R_{P1}C_1 + R_{P2}C_1 + R_{P2}C_2) - g_mL_1L_2R_{P1}R_{P2}C_2]\omega_0^3 - [g_mR_{P1}R_{P2}(L_2 - L_1) + L_1R_{P2} + L_2R_{P1}] = 0 \quad (4)$$

Ultimately, the oscillation frequency can be approximated as follows:

$$\omega_0 \approx \sqrt{\frac{1}{L_2C_2} + \frac{C_1+C_2}{L_1C_1C_2}} \quad (5)$$

In special case when L_1=L_2=L_P and R_{P1}=R_{P2}=R_P, the oscillation frequency in simplified form is as given:

$$\omega_0 \approx \sqrt{\frac{1}{L_P}\left(\frac{1}{C_1} + \frac{2}{C_2}\right)} \quad (6)$$

$$g_mR_P = 1 + \frac{4\left(C_1/C_2\right)^2}{1+2\left(C_1/C_2\right)} \quad (7)$$

It is obvious from (6) that a small variation in C_2 results a large variation in oscillation frequency. In other words, since C_2 has a large coefficient in the nominator, it has more effect on the ω_0 rather than C_1 does. Thus, the capacitor C_2 is realized by varactor resulting a wide frequency tuning range in the proposed current-reuse VCO. Meanwhile, the capacitance C_1 should be very large to have a reasonable tuning frequency at RF frequency of 24GHz. However according to (7), the C_1/C_2 ratio determines the required transconductance for sustainable oscillation. In other words, the higher C_1/C_2 ratio is, the higher transconductance will be. As a result, there is a sever tradeoff between the power consumption and oscillation frequency range of the VCO by tuning C_1/C_2 ratio. Furthermore, the effect of intrinsic parallel resistances in n/pMOS transistors will be reduced by utilizing the parallel-connected C_1 and C_2 network. This network adjusts the output port load impedance of VCO for improving its performance such as phase noise.

As it depicted in Fig. 2, different values of C_1/C_2 ratio are corresponding to certain phase noises. Thus, by finding the optimized value for capacitor ratio, a subtle tradeoff among different features such as power consumption, amplitude imbalance ratio (the ratio of differential output waveforms of V_{out+}/V_{out-}) and phase noise can be reached. As can be seen in Fig. 4, when the capacitor ratio is located in the interval of [1.37 1.73], the phase noise has the minimum value. However in this interval the differential outputs are not symmetry and the amplitude imbalance ratio gets worse. In addition, as the capacitance ratio is low, the power consumption will be low. Thus, by considering the above-mentioned tradeoffs, the optimum point is located in the interval [1.19 1.25].

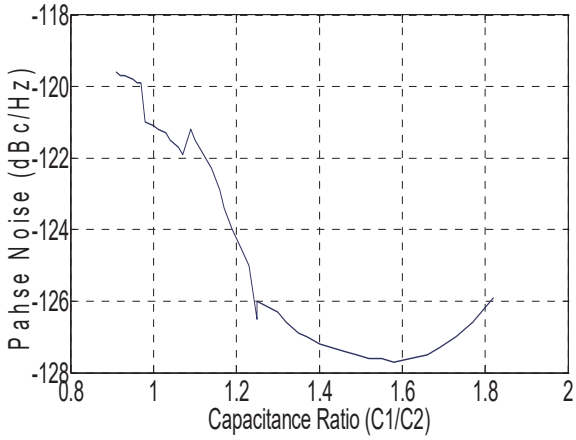


Fig. 4. Simulated phase noise versus capacitance ratio at 1MHz offset frequency.

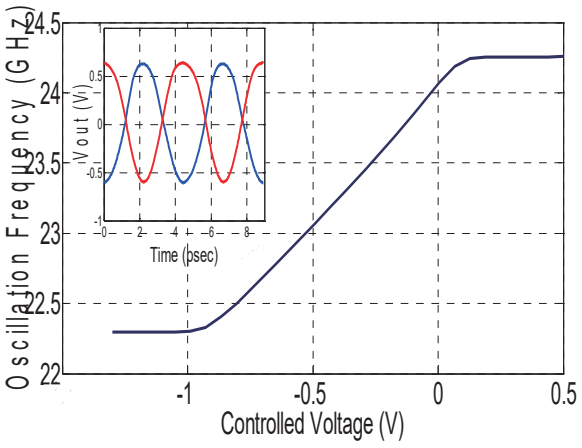


Fig. 5. Measured tuning range and output waveforms of the current-reuse LC VCO prototype.

III. RESULTS AND DISCUSSION

The schematic and die photograph of the proposed current-reuse LC VCO are illustrated in Fig. 2. The proposed VCO consists of n/pMOS transistors in cascode current-reuse configuration to boost transconductance and save current which leads lowering power consumption. While circuit is biased at the supply voltage of 0.95 V, the VCO consumes 321μW. This low power consumption is achieved thanks to low supply voltage and cascode current-reuse structure. In Fig. 3, the oscillation frequency versus tuning voltage is illustrated. The oscillation range from 22.3GHz to 24.3GHz proves that the selection of capacitor C_2 in capacitive-feedback technique as varactor gives an extensively wide tuning range. In Fig. 5, the output waveforms are shown which indicates the imbalance ratio is very small which leads to enhance phase noise of whole VCO.

In the proposed current-reuse LC VCO, a capacitive-feedback technique including capacitances C_1 and C_2 is utilized to enhance the phase noise and to widen the oscillation frequency tuning. As shown in Fig. 6, the source terminal of nMOS swings below than ground and drain terminal of pMOS swings above the supply voltage, due to the in-phase relationship which causes by capacitive-feedback technique and inductors. In other words, due to the charging/discharging among inductors and capacitors, the drain/source voltages of p/nMOS swing above and below than the supply voltage and ground, respectively. To further investigate the oscillation amplitude of the proposed VCO, detailed analysis is provided here.

As explained, the losses in the LC tank represent by R_{Pi} (i=1 and 2). In the steady state region, the output voltages are approximated by $V_{on}=V_{dd}-A\cos(\varphi)$ and $V_{op}=V_{dd}+A\cos(\varphi)$. Here A is the maximum amplitude of VCO and φ is the phase given by $\varphi=\omega_0 t$. The oscillation frequency is given in (4). When voltage gain of nMOS reaches its peak value, the maximum drain current ($I_n(t)$) flows. In pMOS case, the maximum drain current happens when its gate voltage reaches its peak. In other words, when $V_{g,n}= V_{dd}+A$ and $V_{g,p}= V_{dd}-A$, maximum drain currents will occur, respectively. I_0 is the maximum amplitude for the drain current in the verge of V-limited and I-limited regions and it is given in Eq. (8).

$$I_0 \cong \mu_n C_{0x} \frac{W_n}{L}[(V_{dd} + \mathrm{A} + \mathrm{nA} - V_{t,n})(V_{dd} - \mathrm{A} + \mathrm{nA}) - \frac{1}{2}(V_{dd} - \mathrm{A} + \mathrm{nA})^2 \quad (8)$$

where V_t is threshold voltage of MOS transistors, and $n=C_1/(C_1+C_2)$.

The fundamental voltage amplitude of the both positive and negative output ports are expressed in Eq. (9).

$$\mathrm{A} \approx \frac{2}{\pi} I_0 R_o \quad (9)$$

where R_o is the output load of the VCO. After simplification, the output VCO is given as Eq. (10).

$$\mathrm{A} \approx \left(1 + \frac{C_1}{C_2}\right) V_{dd} \quad (10)$$

It is obvious from Eq. (10) that the output amplitude of proposed current-reuse VCO is a function of C_1/C_2 ratio. As can be seen from Fig. 6, by apply the capacitive-feedback technique the VCO output swing is larger than the V_{dd}.

Table I shows performance summary of the proposed LC VCO and comparison with other low power consumption and low phase noise VCOs. As shown in Table 1, the proposed VCO showed lowest power consumption of 0.32mW and an excellent FOM of -204dBc/Hz as compared to recently reported results.

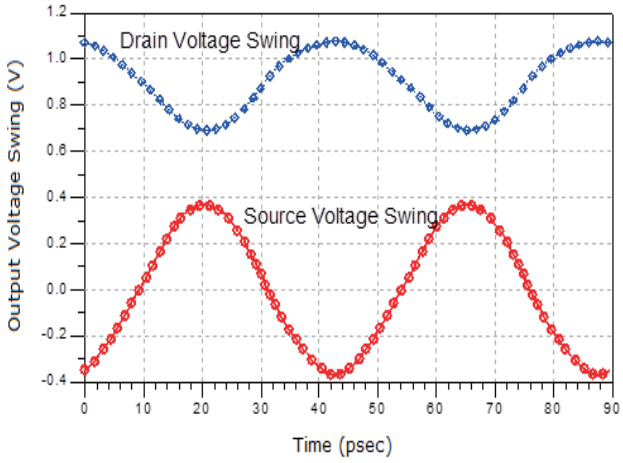


Fig. 6. nMOS source terminal waveform and pMOS drain terminal waveform.

TABLE I.
Comparison of the proposed LC VCO performance and other published works.

Ref.	Tech (nm)	Freq. (GHz)	PN @ 1MHz (dBc/Hz)	P_{diss} (mW)	Area (mm^2)	FOM (dBc/Hz)
[1]	120	44	-101	7.5	0.36	-184.8
[2]	180	5.25	-119	1.9	0.15	-177
[3]	180	2.5	-130.5	2.7	0.36	-191.9
This work	130	24	-123	0.32	0.35	-204

IV. CONCLUSIONS

The 24GHz LC VCO in cascode current-reuse configuration with a very low-power and low-phase noise has been proposed. A capacitive-feedback technique is utilized to enhance output power swing and phase noise. The VCO is implemented in a 65nm CMOS process. The proposed VCO showed lowest power consumption of 0.32mW and an excellent FOM of -204dBc/Hz as compared to recently reported results.

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