A design of Envelope Detector and DC Rectifier for 8~100% ASK Communication

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***Abstract* - The passive multi-mode NFC AFE(Analog Front-End) was proposed and implemented in 65nm CMOS process. We proposed the novelty architecture of DC Rectifier and Envelope Detector which are the most important blocks in passive mode because those generate their own power. The Complementary DC Rectifier is proposed and it is more efficient compared with the conventional DC Rectifier composed of NMOS only or PMOS only. The Envelope Detector generating negative voltage is proposed and it can generate the negative voltage of -0.68V that is used for body bias. The area of the passive multi-mode NFC AFE is 0.19mm×2mm and it is very small compared with the conventional NFC AFE.**

I. INTRODUCTION

Wireless power transfer has broad applications ranging from mobile phone chargers to biomedical implants [1]. NFC (Near Field Communication) is wireless technology that enables the variety of additional services including the transceiver within 20cm at 13.56MHz band and equipped in mobile communication terminal. NFC does not require visual contact, and therefore, it allows more convenient information access [2]. A number of multi-media equipment from digital camera, personal computer, PMP, and MP3 Player to Samsung pay and white pay have adopted the NFC technology lately. [3] ISO (International Organization for Standardization) sets the various standards of NFC and RFID depending on types and modulations based on the standards as shown in TABLE I [3-5].

TABLE I
Modulation specification of 13.56MHz RFID and NFC

ISO Standard	Modulation (Reader to Tags)
14443 A	100% ASK
14443 B	10% ASK
15693	10% or 100% ASK
18092	8~30% ASK (Passive) 100% ASK (Active)

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ASK (Amplitude Shift Keying) modulation on TABLE 1 is adopted in many communication systems such as NFC and RFID (Radio Frequency Identification) [6]. As ASK modulation is different based on ISO standard types, different circuit should be used when the signal is demodulated from Tag. Tag takes charge of demodulation in analog part and memory is in charge of digital part. Analogue part has its own power supply when Tag is on active mode. However, on passive mode, if signal is sent wirelessly from the Reader, the power is self-generated by coupling through antenna made of inductor. Therefore, the role of AFE (Analog Front-End) is very important on passive mode. AFE block includes the low-voltage bandgap, the LDO (low-dropout regulator) with the bias-boosted gain stage, and the adaptive dc limiter [2]. This paper proposed the AFE part that can demodulate every signal with ASK 8~100% modulation using 65nm CMOS process and verified its operation with the chip measurement.

The remainder of this paper is organized as follows. In Section II, the proposed passive multi-mode NFC Tag design is presented. The post-simulation results are described in Section III and experimental results are provided in Section IV. Finally, the conclusion is given in Section V.

II. PASSIVE MULTI-MODE NFC TAG DESIGN

A. DC Rectifier

The AFE block diagram of the proposed passive multi-mode NFC Tag is shown in Fig. 1.

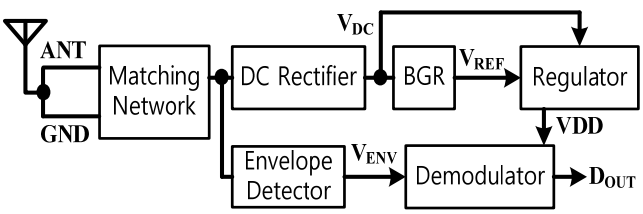


Fig. 1. AFE block diagram of the proposed passive multi-mode NFC Tag

When the Reader antenna and Tag antenna are within 10cm, signals are emitted by inductor coupling of Tag antenna. The Emitted signal goes through matching network and is transmitted to the DC rectifier and the envelope detector without any loss. The DC rectifier is the first block

to generate power supply for Tag on passive mode. The incoming signal with amplitude changing depending on ASK modulation ratio is received and corrected into the relatively steady DC 2V voltage. In BGR (Band-Gap Reference), DC Rectifier output, V_{DC} is applied and relatively steady DC 0.67V is generated without the dependency to the surrounding temperature change. The regulator receives V_{DC} and BGR output, V_{REF}, and creates the steady 1V DC that can operate with the demodulator and digital part. The Envelope detector output, V_{ENV}, and the regulator output, VDD, are entered to the demodulator and the demodulator demodulates the emitted signal to antenna. The conventional DC Rectifier circuit and the proposed complementary DC Rectifier circuit are shown in Fig. 2 [7-8].

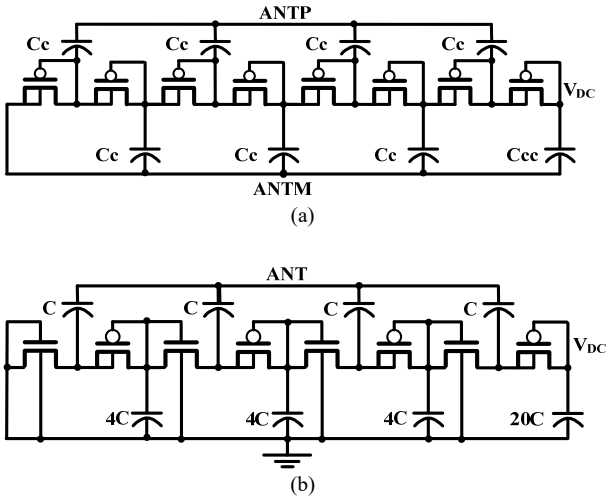


Fig. 2. (a)Schematic of conventional DC Rectifier (b)Schematic of proposed Complementary DC Rectifier

The difference from the conventional circuit is that by applying –VDD voltage, not 0V, to inverter VSS and NMOS source, the ripple is reduced in negative supply.

The proposed complementary DC Rectifier was designed to have 4 stages. The difference from the conventional circuit is that PMOS and NMOS pair, not just one type of MOS, were used for diode. For PMOS output which is slower than NMOS output, capacitors are 4 times larger than the one connected to NMOS output connected and delayed the discharge time. The signal amplitude becomes smaller when the data is "LOW" on ASK modulation, though V_{DC} does not go down until it reaches the desired level and the steady DC voltage output, the capacitor on the last stage was designed which is 20 times larger than the minimum size. The proposed Complementary DC Rectifier takes up the smaller space than the conventional circuit and shows the steady output voltage.

B. Envelope Detector

Envelope Detector is used in various ways such as ET (Envelope-Tracking), AM radio receiver, and so on [9]. The schematic of conventional Envelope Detector and the proposed Negative Voltage Generating Envelope Detector are shown in Fig. 3 [10].

As the proposed Tag has one input signal, ANT, it was designed to have single input compared with the conventional circuit. Also, the resistance, R_{ENV}, was added beside the capacitor, so the amplitude of V_{ENV} was increased by 55% compared with the conventional Envelope Detector that has no resistance [10]. Also, when ASK modulation is applied in Modulator block and the answer signal was sent through antenna, as shown in Fig 2, minus voltage called V_{DCM} can be generated to use –VDD to increase the output amplitude. After the simulation, maximum V_{DCM} was 0.68V.

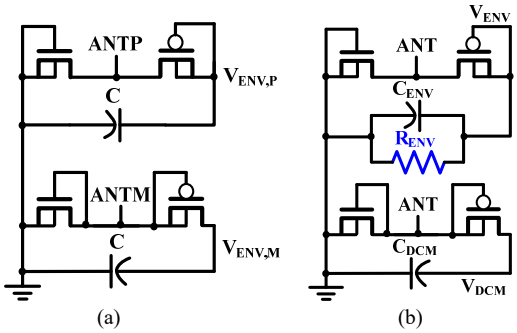


Fig. 3. (a)Schematic of the conventional Envelope Detector (b)Schematic of the proposed Negative Voltage Generating Envelope Detector

C. Voltage Limiter

The NFC Signal of 13.56 MHz is received via the NFC antenna and generates the DC voltage through the DC Rectifier. The DC Rectifier in this paper is the Voltage Multiplier structure and it is composed of 4 stages to increase the distance between NFC Reader and NFC Tag. It could be possible to generate the stable DC voltage even though low voltage is applied. But if the distance between the NFC Reader and NFC Tag is short and tag generates the large DC voltage, it may cause damage to the internal circuitry like Bandgap Reference, LDO Regulator. the Voltage Limiter is required to prevent damages to the internal circuit and its schematic is shown in Fig. 4.

When the output voltage of DC Rectifier is lower than the sum of the threshold voltage with M2, M3, M4, the current does not flow through the R, so M1 is off. If the output voltage of DC rectifier is higher than the sum of the threshold voltage of the M2, M3, and M4, the current flows through R, so it turns on of M1. The large size of the NMOS which is turned on is large when the current is discharged.

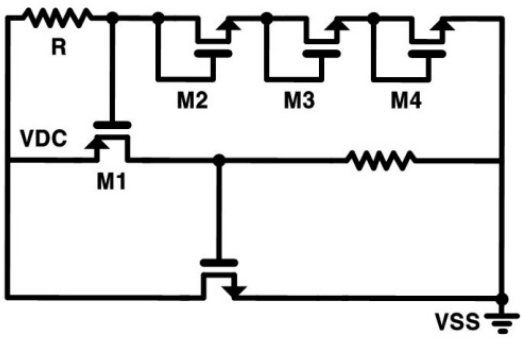


Fig. 4. Schematic of the Voltage Limiter

D. BGR, Regulator

The conventional circuit of BGR and Regulator was used in this design, and those circuits were modified suitable for 65nm process and its schematics are shown in Fig. 5 [11]. The amplifier used in BGR and regulator was designed to have two amplification stages and the PNP transistor used in BGR is implemented in CMOS process using N-well.

Because the regulator output is easily changed according to the external temperature and environment, the output of the voltage Multiplier (V_{DC}) is inappropriate as the power source for the internal circuit. The BGR circuit is suitable, because the output voltage is not sensitive to the changes in external temperature and environment.

Through the combination of V_{ptat} (Proportional to absolute temperature) and V_{ctat} (Complementary to absolute temperature), BGR can make the constant voltage insensitive to temperature.

The voltage that decreases with the temperature (V_{ctat}) can be obtained in the voltage across the diode. (Fig. 6.) To obtain the negative coefficient, the derivative of $V_D = V_T \times \ln(\frac{I_0}{I_s})$ is used.

$$\frac{\partial V_D}{\partial \mathrm{T}} = \frac{\partial V_T}{\partial \mathrm{T}} \times \ln\left(\frac{I_0}{I_s}\right) + V_T \times \frac{\partial (ln\frac{I_0}{I_s})}{\partial T}$$

$$\frac{\partial V_D}{\partial \mathrm{T}} = \frac{\mathrm{K}}{\mathrm{q}} \times \ln\left(\frac{I_0}{I_s}\right) - V_T \times \frac{1}{I_s} \times \frac{\partial I_s}{\partial T}$$

$$\frac{\partial I_s}{\partial \mathrm{T}} = I_s \times \left(\frac{E_g}{KT^2} + \frac{4+m}{T}\right), \mathrm{m} = -\frac{3}{2}$$

$$\therefore \frac{\partial V_D}{\partial \mathrm{T}} = \frac{V_D - (4+m) \times V_T - \frac{E_g}{q}}{T}$$

Substituting constants in the above equation, We could obtain the coefficient, $-1.6\mathrm{mV}/\ ^{\circ}\mathrm{K}$.

The voltage that increases with the temperature (V_{ptat}) is shown in Fig. 7. When assumed that the same current (I_0) flows, V_{ptat} can be determined by the area ratio of the two diodes.

$$V_D = V_T \times ln\frac{I_0}{I_s}$$

$$V_{D1} = V_T \times ln\frac{I_0}{n \times I_s} \ (\text{n= The number of Diodes})$$

$$\therefore V_D - V_{D1} = V_T \times \ln(n)$$

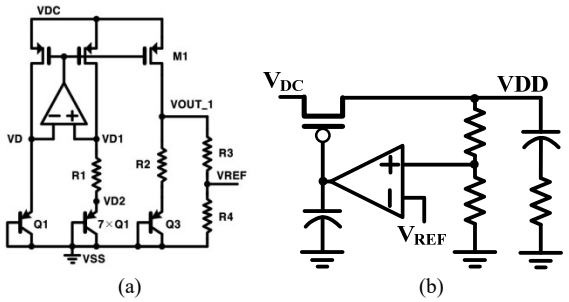
In Fig. 5. (a), with the addition of the R1

$$V_D = I_0 \times R1 + V_{D2}$$

Copying the PTAT current by the addition of M1, and R2

$$\therefore V_{out} = \frac{R2}{R1} \times V_T \times \ln(n) + \frac{\partial V_D}{\partial T}$$

The regulator generates output through the input BGR reference output voltage and feedback of output voltage.



(a) (b)

Fig. 5. (a) Schematic of BGR (b) Schematic of Regulator

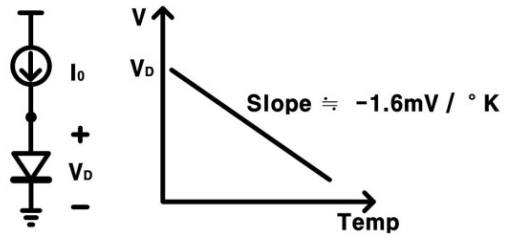


Fig. 6. Voltage of CTAT

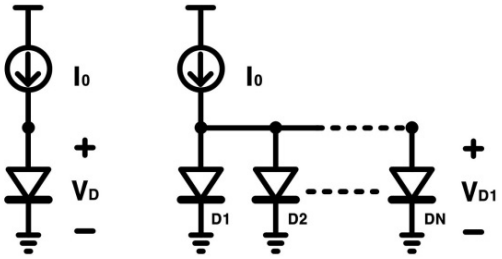


Fig. 7. Voltage of PTAT

E. Demodulator

The demodulator used the conventional circuit in this design and its schematic is shown in Fig. 8 [12]. In Fig 8, V_{ENV} is the first input but starts to operate after the regulator output, VDD, is entered. V_{REF} goes through unit gain buffer and is the input on amplifier and schmitt trigger block. V_{ENV} goes through RC filter and only the rising edge and falling edge signals are entered to amplifier [12]. The rising edge and falling edge are entered to the Schmitt trigger block and The Schmitt trigger demodulates them into square wave [12].

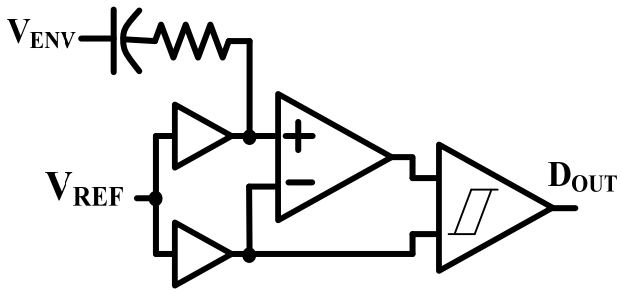


Fig. 8. Schematic of demodulator

F. Load Modulator

The Load Modulator circuit is shown in Fig. 9.
It is composed of a NMOS and a MOS Capacitor. When the gate of the NMOS receive the response signal of 847KHz from the Digital Block, it is connected the drain of the MOS connected antenna with the the source of the MOS connected MOS capacitor, and it changes the amplitude of Reader signal.

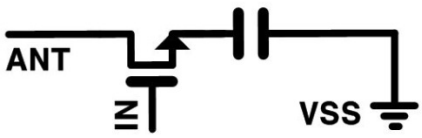


Fig. 9. Schematic of Load Modulator

G. Power-On Reset

The Power-On Reset circuit used in this work is shown in Fig. 10. The circuit for resetting the Digital Block after sending and the response data between the Reader and the Digital Block is the Power-On Reset. It is composed of MOS Capacitor and Schmitt Trigger.

The output voltage of the DC Rectifier was used as the supply voltage of the Power-On Reset. The current mirror to control the amount of current was used on a Stage-3.

Since the input of the Schmitt Trigger and the MOS Capacitor is connected, the current applied through the current mirror determines the reset wait time until capacitor charging voltage goes a high switching point of the Schmitt Trigger.

After the reset, the data doesn't come from the Reader and the MOS capacitor become discharge state. This makes the switching point of the Schmitt Trigger pull down, it is possible to reset the high switching point when sending the data again.

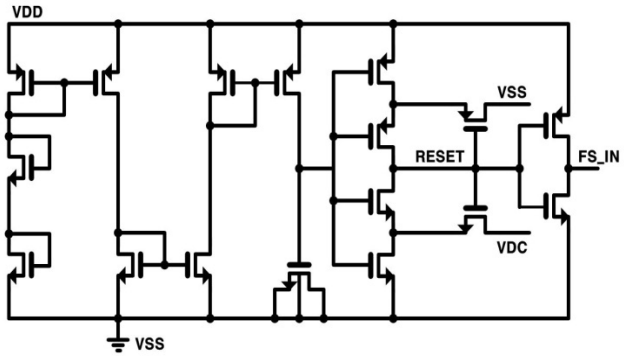


Fig. 10. Schematic of Power On Reset

III. SIMULATION RESULTS

The proposed passive multi-mode NFC Tag was designed using 65nm CMOS process and CADENCE Spectre was used for the verification. Fig. 6 is the simulation results of the minimum input amplitude condition, so the proposed Complementary DC Rectifier can operate around this value. DIN is the input data with 847 kHz speed, which is the highest data speed on ISO/IEC 18092 standard.

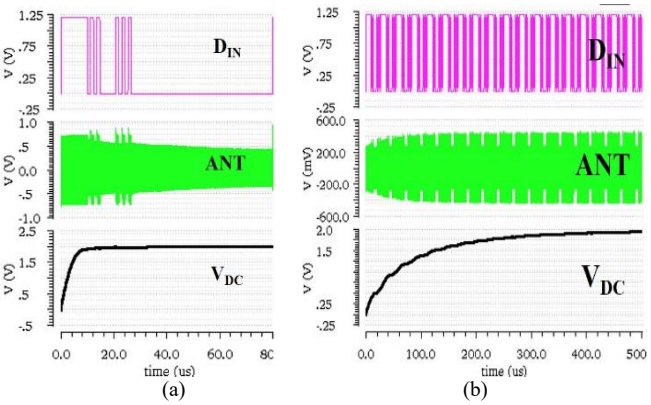
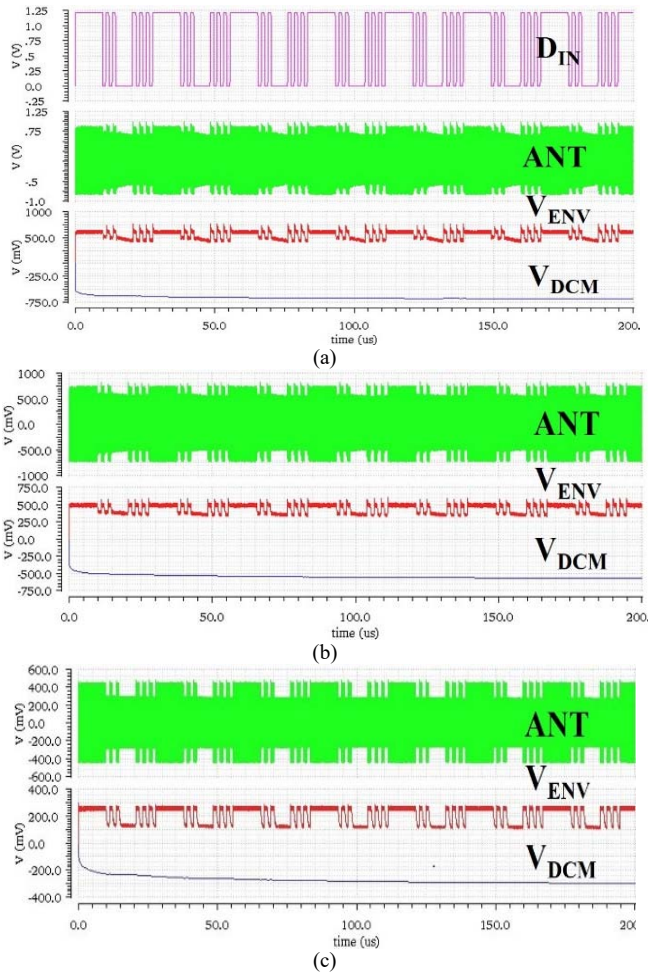
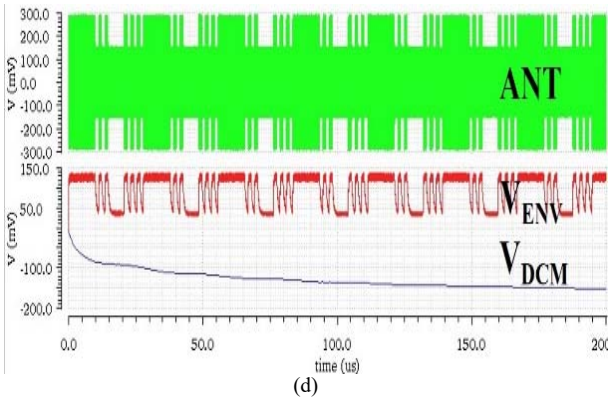


Fig. 11. Simulation result of VDC versus input amplitude (a)1.6V (b)0.8V

In Fig. 11, it was confirmed that the amplitude of emitted voltage in antenna is larger than 2V if DC Rectifier reaches 0.8V and higher. It also shows that V_{DC} maintains its value when the data is low, and goes to 2V when the data is high.

The simulation results of the proposed Negative Voltage Generating Envelope Detector depending on ASK modulation value are shown in Fig. 12. By the simulation, it shows that 8~30% ASK modulation specifications were satisfied using the proposed IC.





(d)

Fig. 12. Simulation result of VENV and VDCM versus ASK modulation ratio (a)8% (b)10% (c)20% (d)30%

Fig. 13 is the simulation result of the DC Rectifier according to time, where the Rectifier uses NMOS only, PMOS only, and where it is designed using complementary structure. Where only PMOS is used, the DC output voltage generated by the circuit is lower than other structure circuits where only NMOS is used, the circuit produced the DC output which is close to the complementary structure, but the charging time of NMOS structure is slower than the complementary structure.

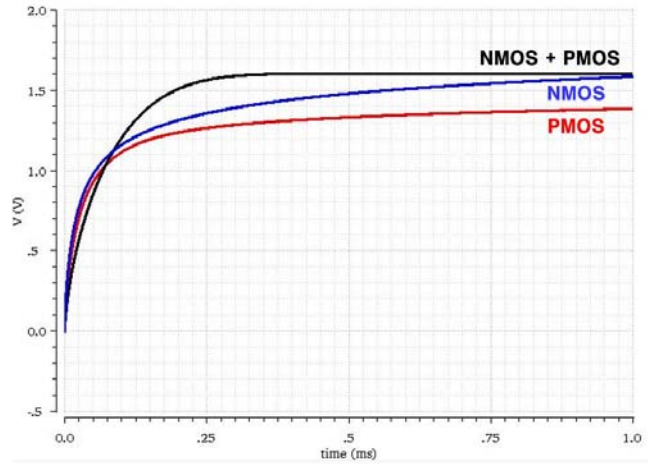


Fig. 13. Simulation result of DC Rectifier with NMOS and PMOS selection

Fig. 14 shows the simulation result between the envelope detector with and without resistance R_{ENV}. After the simulation, it showed that the proposed circuit operates well compared to the previous works [10].

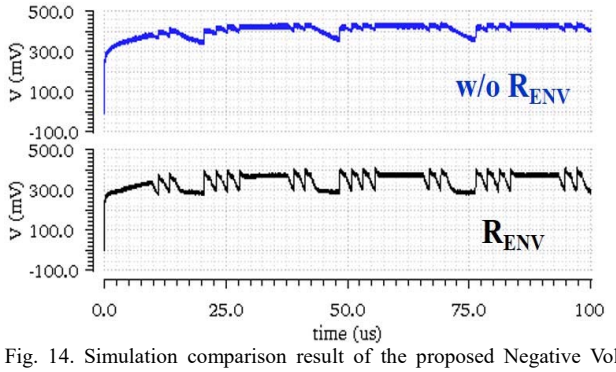


Fig. 14. Simulation comparison result of the proposed Negative Voltage Generating Envelope Detector and conventional Envelope Detector

The simulation results of the operation of BGR, Regulator, and Demodulator are shown in Fig. 15. According to the simulation, it shows that the waveform was demodulated correctly by the steady V_{REF} voltage.

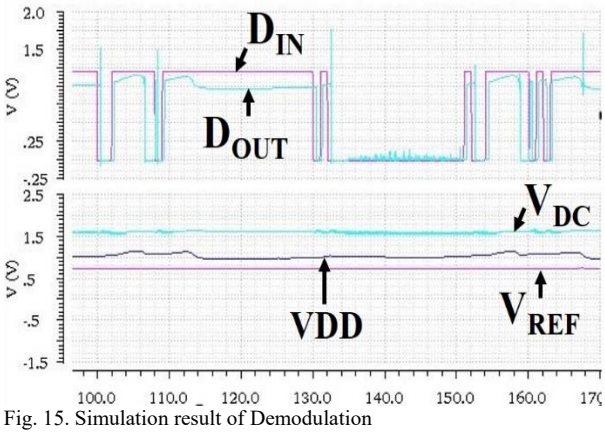


Fig. 15. Simulation result of Demodulation

Fig. 16 is the simulation result of the Power supply consist of DC Rectifier, Bandgap Reference, LDO Regulator and Power-On Reset.

The ASK signal of Modified Miller coding, RX_IN coming from the Reader goes in the DC Rectifier. It makes the output voltage VDC. The Voltage Limiter did not work because the voltage of the ASK signal (RX_IN) which is entering is low at this simulation.

Power-On Reset and Bandgap Reference is supplied with the output voltage of DC Rectifier (VDC). The Bandgap Reference outputs the constant voltage (VREF) and Schmitt Trigger operates the reset function (POR_RST) after passing the charging time of the high switching point of the Schmitt Trigger.

After the LDO Regulator receives the VREF from the Bandgap Reference, VREG can be obtained through the Error Amplifier operation. It is used as the Power supply voltage (VDD) of the NFC Analog Front-End.

Fig. 17 is the simulation result of Demodulation operation. The ASK signal of Modified Miller coding, RX_IN coming from the Reader enters the proposed Envelope Detector for ASK 8 ~ 100% Modulation. RX_IN is modulated ASK 100% in this simulation. VREC is the output of the Envelope Detector. VREC is passed through the filter, which enters the one input of the Comparator. The other input of the Comparator receives the VREF, the Comparator output (OUT_FILTER) is generated around the VREF. A comparator receiving the OUT_FILTER and VREF is connected to the Schmitt Trigger, which produces the demodulated Signal, OUT_DEMOD.

OUT_DEMOD goes to the passing the buffer for the Digital Block. This operation is done by the PAD in this design. the Digital Block received the data through the operation of demodulation and sends the response signal.

The Response signal of Manchester coding has the carrier frequency of 847 KHz. Receiving the response signal can watch that the amplitude of the RX_IN moving at the rate of 847 KHz.

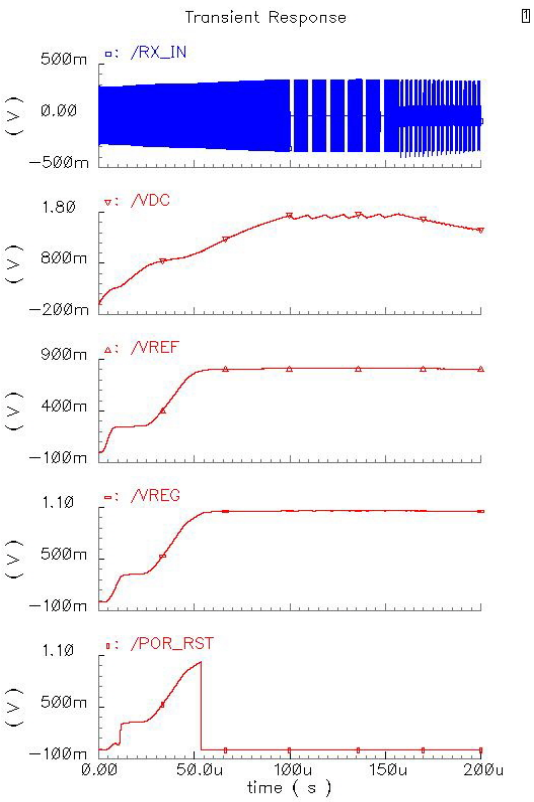


Fig. 16. Simulation result of Power Supply

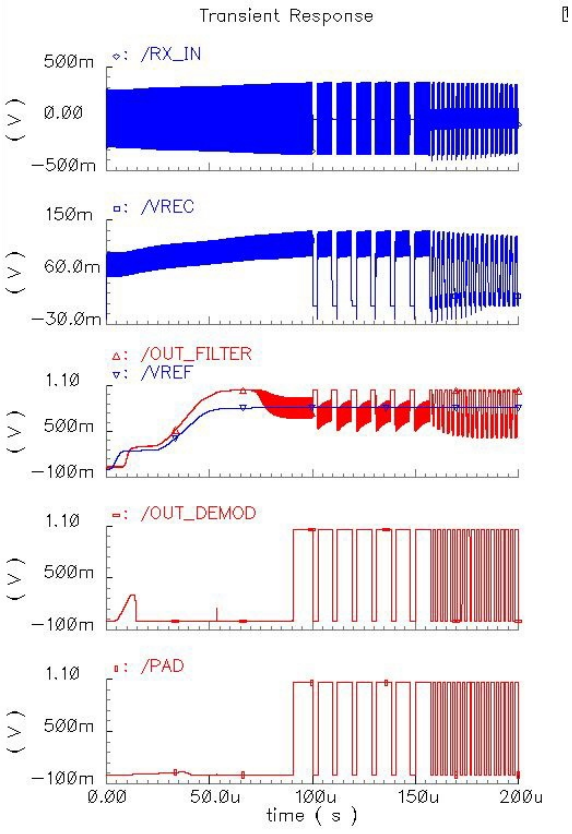


Fig. 17. Simulation result of Demodulation.

IV. MEASUREMENT RESULTS

The chip measurement was conducted using the probing test process in probe station and connection with the antenna implemented with the resonant frequency of 13.56 MHz. The size of the implemented chip is 1.9mm×2mm and the chip microphotograph is shown in Fig. 18.

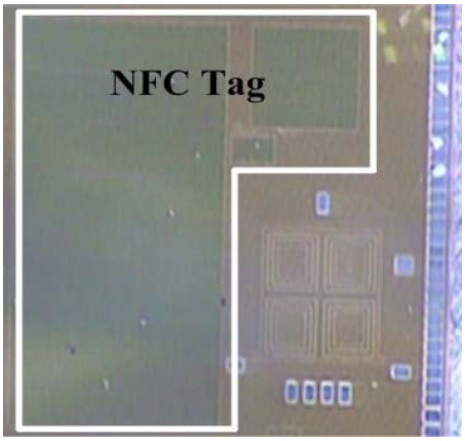


Fig. 18. (a) Chip microphotograph

The proposed NFC AFE receives the signals from the Reader antenna by connecting the antenna to input terminals. The Tag antenna and Reader antenna should be placed within 10cm distance. The Reader sends the regular signals for Tag with the programmed communication protocols. Depending on ISO standard, the different waveforms with ASK 8% to 100% could be sent. The pictures of chip measurement and test result are shown in Fig. 19 and Fig. 20. respectively.

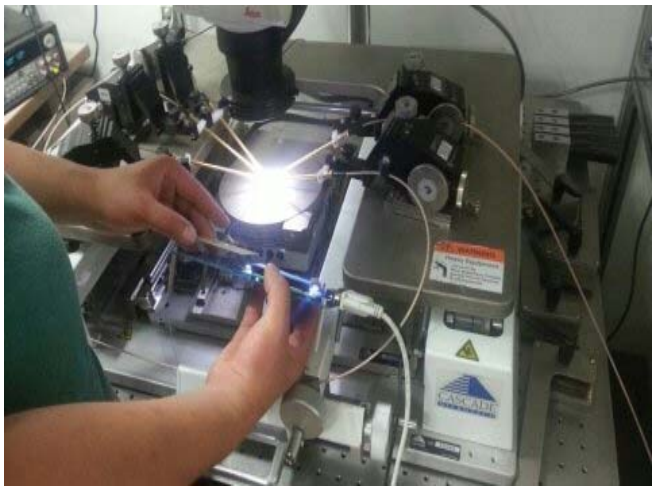
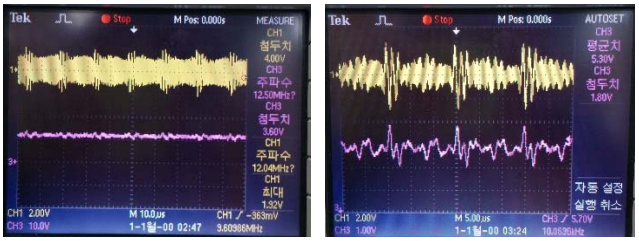
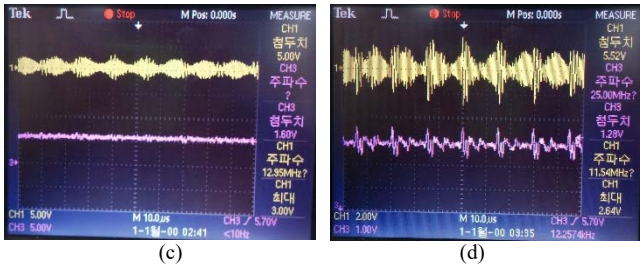


Fig. 19. Measurement environment of the proposed passive multi-mode NFC AFE



(a) (b)



(c) (d)

Fig. 20. Measured waveforms of passive multi-mode NFC AFE versus ASK modulation rate of reader (a) 8% (b) 30% (c) 50% (d) 100%

After the chip measurement, it shows that the demodulation operation is verified using the designed chip.

V. CONCLUSIONS

The Envelope Detector and DC Rectifier for ASK 8~100% Signal are proposed and implemented in 65nm CMOS process. The NFC AFE has many blocks like DC Rectifier, Envelope Detector, BGR, Regulator, Demodulator, and so on. We proposed the novel architecture of DC Rectifier and Envelope Detector that are most important blocks in passive mode Tag because those generate their own power. The Complementary DC Rectifier is proposed and it is more efficient compared with the conventional DC Rectifier composed NMOS only or PMOS only. The Negative Voltage Generating Envelope Detector is proposed and it can generate the negative voltage of -0.68V that is used for MOSFET body bias. The area of the NFC AFE is 0.19mm × 2mm and it is very small compared with the previousely reported NFC AFE.

Since the proposed passive NFC AFE Tag has high efficiency in power and small area, it is feasible to use the proposed tag for NFC applications for various wireless communication systems.

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