Nonlinearity analysis of 65nm 8bit Vernier Time-to-digital Converter

Hyun Min Koh
Department of Electrical Engineering, Yonsei University
E-mail: hmkoh728@yonsei.ac.kr

***Abstract* - This paper analyzes the nonlinearity of Time-to-Digital Converter (TDC) used in wireless bearing angle measure system by using Integral Non-Linearity (INL) and Differential Non-Linearity (DNL) specification. Nonlinearity can be represented by the distance error, which indicates the uncertainty of the angle and position in this system. We investigate the distance error based on INL and cause of nonlinearity from the viewpoint of layout. We compare pre and post layout simulations of parasitic resistance in metal power line, underlying important layout points. Jitter and mismatch simulation are proposed for setting delay buffer size and TDC time resolution. Wire bonding inductance simulation is also considered for checking robust circuit operation. Verified TDC is an 8bit with a 18ps resolution. The measured DNL and INL were 0.8 LSB and -15 LSB. The simulated TDC is fabricated through Samsung 65nm chip process.**

***Keywords*—Angle sensor, Localization, TDoA, Time to Digital Converter**

I. INTRODUCTION

Location information is widely used in indoor office space, public place, hospital and industries. Among various methods for obtaining indoor location information, ultra-wideband (UWB) technology is particularly popular [1,2]. UWB is a wireless communication method using unlicensed ultra-wideband of 3-10GHz. It can be implemented with low power and it is strong against multipath interferences because impulse waveform exists only for a short time in times series.

Fig.1 is a diagram of typical wireless system for bearing angle measure between transmitter and receiver. The receiver can be largely divided into two parts. One is the analog front-end (AFE) stage that amplifies the received small signal in Fig.2, and the other is the time-to-digital converter (TDC) stage that detects the time difference between two received signals START and STOP in Fig.4 [3,4].

At the analog front-end stage, the small waveform signal transmitted from Tx is amplified and the edge of the waveform is extracted by the envelope detector. Finally, comparator makes the arrival point of received signal into one square wave pulse.

The time difference of the received pulse occurs between two receivers Rx_1 and Rx_2. TDC detects time difference and outputs it as eight bits. the distance difference can be achieved by multiplying the time difference (TD) by the speed of light (c) in Fig.3 and interval of Rx1 and Rx2 is already known. Therefore, the bearing angle(θ) can be obtained by inverse cosine as (1). Finally, the TX (target) position can be determined by using intersection of several bearing angle information [5].

TDC is a core circuit block in this bearing angle measurement system. Since nonlinearity causes distortion in the distance difference, high linearity TDC is required for accurate bearing angle measurement.

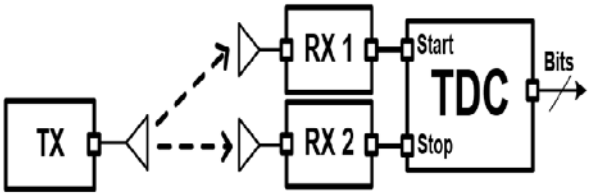


Fig.1. Bearing angle measurement system diagram

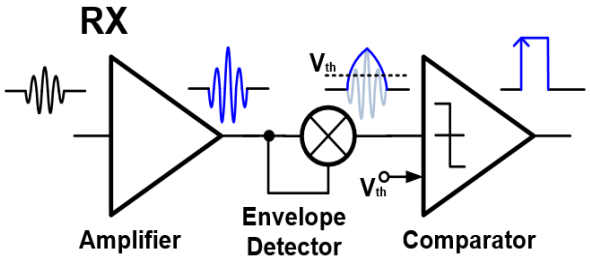


Fig.2. Analog front end receiver diagram

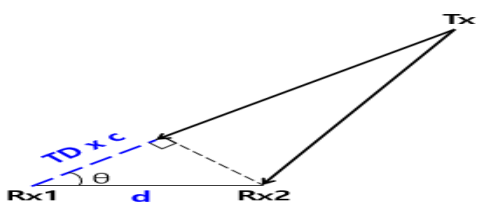


Fig.3. Principle of bearing angle measurement

a. Corresponding author; hmkoh728@yonsei.ac.kr

Manuscript Received Aug. 11, 2018, Revised Sep. 09, 2018, Accepted Sep.18, 2018

$$\theta = \cos^{-1}\left(\frac{TD \times c}{d}\right) \quad (1)$$

II. EXPERIMENTS

A. Concept of Vernier TDC

TDC converts time difference into digital bits and consists of a delay line and a thermometer to binary encoder as shown in Fig.4.

Vernier delay line measures the distance using the delay difference of the START and STOP delay buffer, thus achieving a finer resolution than a structure using one delay line known as flash TDC [6]. The delay difference between START and STOP line is implemented by changing the channel width, because the low to high (or high to low) transition time of inverter is proportional to the capacitance and is inversely proportional to VDD and channel width. The larger the channel width is, the more current flows and the faster delay can be realized.

The smaller the delay difference between START and STOP buffer, the finer time resolution can be achieved. However, the dynamic range is reduced. In other words, time resolution and dynamic range are inversely related.

Thermometer to binary encoder converts the 256 thermometer codes into digital bits. Thermometer codes can be obtained from the SR latch (arbiter, early-late detector), and the SR latch is connected to each delay buffer to determine which of the START and STOP signal has arrived first.

B. TDC simulation

Fig.5 is the simulation result of the timing diagram in Fig.4. The left side shows the simulation result where the START and STOP signals pass each delay buffer, and the right side shows the output of the corresponding SR latch.

At the first time, the START signal arrives before the STOP signal. In 7th delay buffer, the START signal is caught by the STOP signal. The SR latch output is 1 until the START and STOP signals are reversed. The SR latch outputs of the remaining delay buffers are all 0 after being caught. Just as the thermometer increases from the beginning to a certain temperature, the thermometer code increases from the beginning until the START and STOP signals are reversed.

The delay of the START buffer is 32ps, and the delay of the STOP buffer is 18ps. Therefore, the time resolution in simulation result is 14ps. In simulation testbench, START and STOP signals are put into the input with a 90ps time difference. Since the decimal of thermometer code is 6, TDC result estimate the START and STOP time difference to 84ps.

C. TDC measurement setting

Fig.6 shows TDC measurement setting. Data timing generator generates START and STOP signals with certain time difference and logic analyzer represents 8bit which is the TDC output value. We synchronized the data timing generator and logic analyzer and automated measure process using Labview.

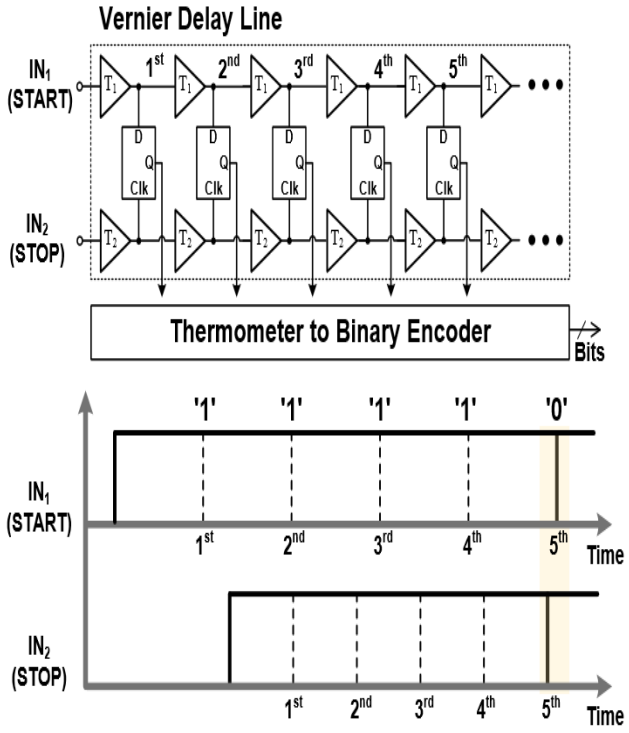
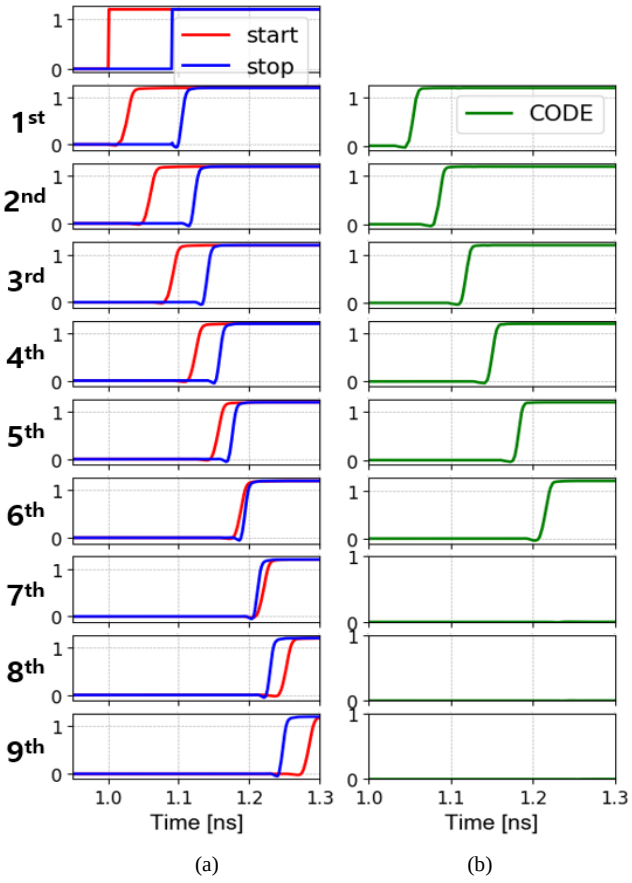


Fig.4 TDC block and timing diagram



(a) (b)

Fig.5. TDC timing simulation (a) START and STOP signal, (b) Thermometer code

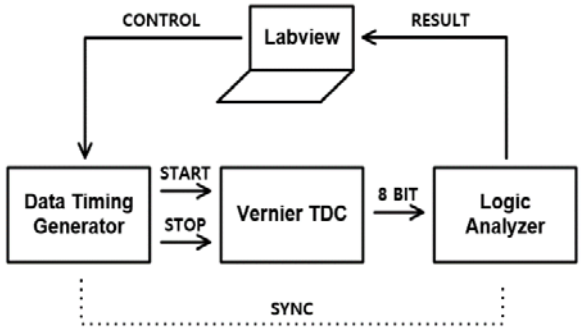
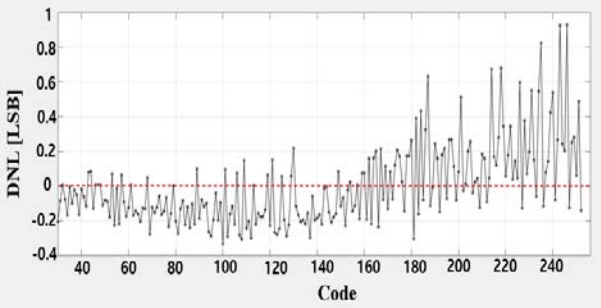
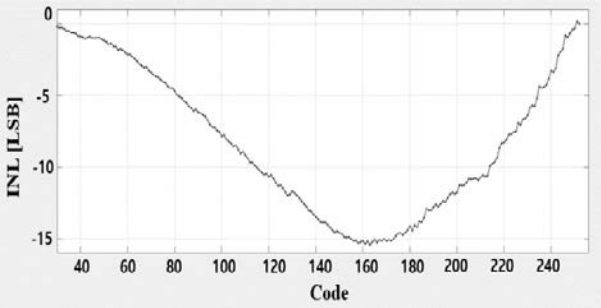


Fig.6. TDC measurement setting



(a) DNL



(b) INL

Fig.7. measured DNL & INL

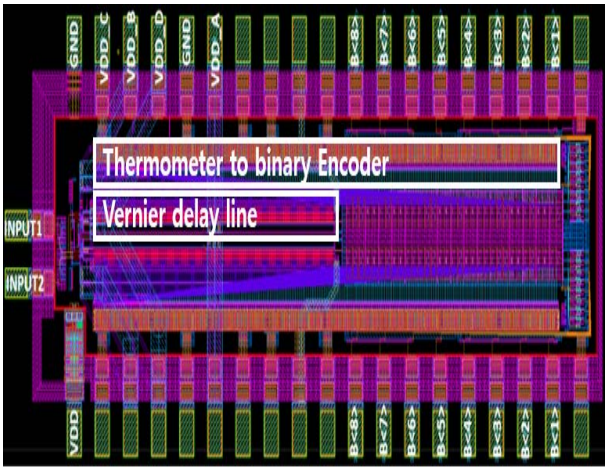


Fig.8. TDC Layout

III. RESULTS AND DISCUSSIONS

A. Linearity of TDC

The linearity of the TDC has been measured in terms of differential-non-linearity (DNL) and integral-non-linearity (INL). DNL is an error of each step from its average value (2), and INL is an error of the step position from its average value (3). In Fig.7 the measured DNL is -0.38 to 0.8 LSB and the INL is -15.3 to 0.2 LSB. The measured DNL sharply degrades after half the delay line.

$$DNL = \frac{measured\ \ delay - average\ \ delay}{average\ \ delay} \quad (2)$$

$$INL = \sum_{n=1}^{n=256} DNL_n \quad (3)$$

In TDC with 18ps resolution, 1 LSB error causes a 5.4 mm distance error, and -15 LSB error in INL finally results in 8 cm or more distance error.

B. TDC layout

Fig.8 shows the layout of the TDC, and it was confirmed that the parasitic resistance of the power line was the cause of the nonlinearity in Fig.7. We review several mistakes in the power line layout and verify this by pre and post layout simulation.

To reduce mismatch between transistors, which causes nonlinearity, the following points should be noted during layout [7]. Keep the channel width, number of fingers, and the channel length of the transistor as equal as possible and attach the delay line as closely as possible. If the delay line spacing is wide, parasitic capacitance and resistance are generated on the metal line interval between two delay buffers. Since the transistors are affected by temperature and other environmental changes such as noise, it is important to reduce such variations between each transistor by placing each delay buffer as tightly as possible. To densely attach the transistors, sharing the source (or drain) of two transistors or using the flatten function to remove unnecessary parts from

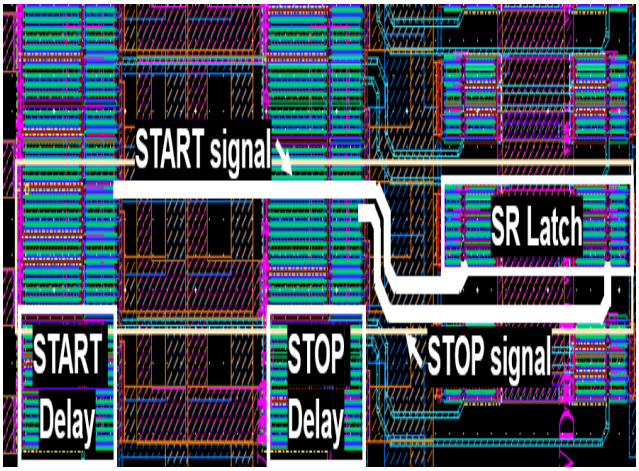


Fig.9 Asymmetry and non-uniform start and stop signal lines

the built-in transistor can be considered. It is also possible to arrange a dummy at the end of the delay line to suppress mismatch due to asymmetry at the end of the transistor.

The time delay is more influenced by the capacitance than by the resistance. Therefore, it is important to reduce the capacitance component of the transistor and signal line. The larger the number of transistor finger, the smaller the resistance of the transistor gate. However, as the number of transistor finger increases, the transistor area increases and causes a larger capacitance. Therefore, the number of fingers was two for the symmetry of the PMOS source, and the channel width per unit finger is changed depend on START or STOP line.

When the length of the metal line is constant and the width of the metal line in the layout increase, resistance in metal line decrease and the capacitance in metal line increase. Therefore, for the signal line connecting each delay buffer, the minimum metal width was used to reduce the effect of the capacitance rather than the resistance. Since the capacitance is inversely proportional to distance, using upper metal layer can reduce capacitance near signal line.

The most important point in TDC layout is the symmetry of the START and STOP delay lines. In Fig.9, START and STOP signal lines applied to the SR latch have different length and asymmetry. Timing offset can occur in different signal length and asymmetry. This problem can be solved by placing an SR latch between the START and STOP delay buffer or placing SR latch line parallel to the each START and STOP line side by side.

START, STOP, and SR latches were laid out in one delay unit. If certain circuit blocks are repeated in layout such as delay line, these repeated blocks can be bound to layout unit and it gives greater efficiency when the repeated blocks are modified.

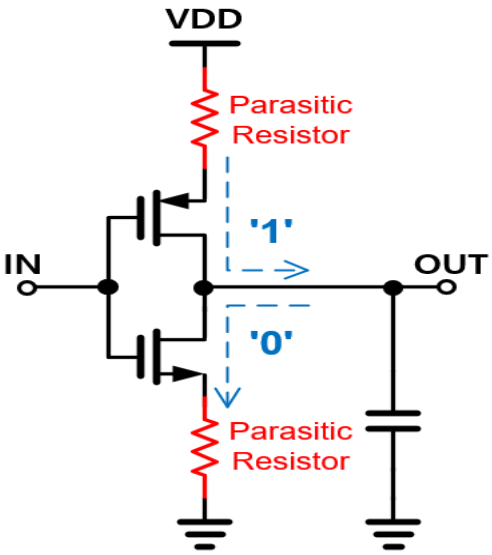


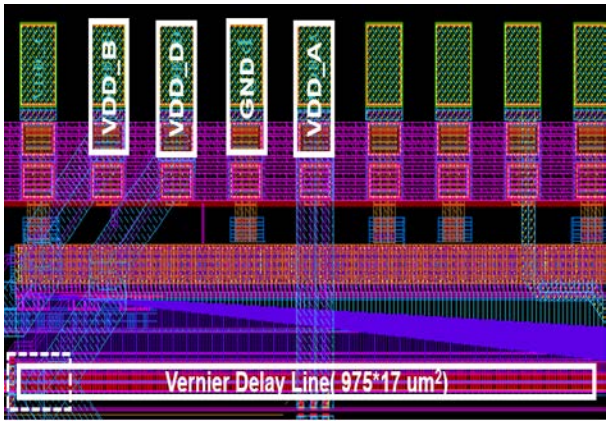
Fig.10. RC delay caused by parasitic resistance

C. Verification of Powerline Layout

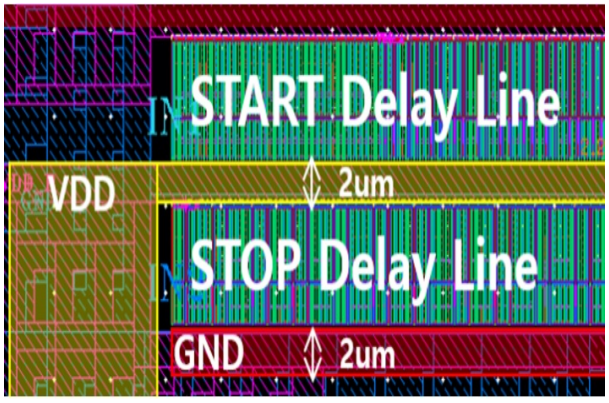
Mistakes in the power line layout cause parasitic resistance as shown in Fig.10. The parasitic resistance in the power and ground of the inverter delay cell causes RC delay with load cap during pull down or up state. RC delay makes serious distortion in uniform time delay. The parasitic resistance in the delay line is more problematic because the small parasitic resistances accumulate along the delay line and cause a greater adverse effect.

Fig.11 shows the failure examples of power line layout. In (a), VDD and GND supplied from the pad are not applied uniformly to the delay line but applied to only a specific portion. Since the only one metal layer is used, parasitic resistance can be induced. In (b), when the width of the metal line is narrower than the metal length, a large parasitic resistance occurs due to the sheet resistance.

The sheet resistance can be obtained by using the width (W) and the length (L) of the metal line. In Fig.11 (b), the length and width of the power line are 2000um and 2um respectively, and it has 1,000 sheet resistance. There are about 250 delay buffers in 8bit delay line, four sheet resistances occur between each delay buffer. Considering the one sheet resistance of the lowest metal layer, it can be assumed that about 400mΩ parasitic resistance occurs between each delay buffer.



(a)



(b)

Fig.11. Layout failure in power line (a) Problems of using one metal layer from pad and partially supplied power (b) problem of Narrow power line width

This can be simulated as shown in Fig.12 through the schematic model, and the result is shown in Fig.13. The cross function of Specter Calculator is used to extract the points that intersect with a specific threshold voltage value on the time axis and the time resolution, DNL and INL characteristics of the TDC can be obtained. In pre-layout simulation with parasitic resistance modeling, the DNL is -0.2 to 0.28 LSB and the INL is -17.5 to 1.9 LSB. In post-layout simulation, the DNL is -0.4 to 0.25 LSB and the INL is -27 to 1.4 LSB. The nonlinearity tends to be sharply decreased as the number of delay buffer increases. The accumulation of parasitic resistances causes this nonlinearity and shows a similar tendency when compared with the measured values in Fig.7.

Parasitic resistance can be minimized by using an upper metal layer which has small sheet resistance or by overlapping several metal layers and supplying power at both ends of the delay line which has the effect of making the sheet resistance look parallel.

The power line should be configured in a branch structure which provides a variety of ways for power, so that supplied power can be evenly distributed over long delay line.

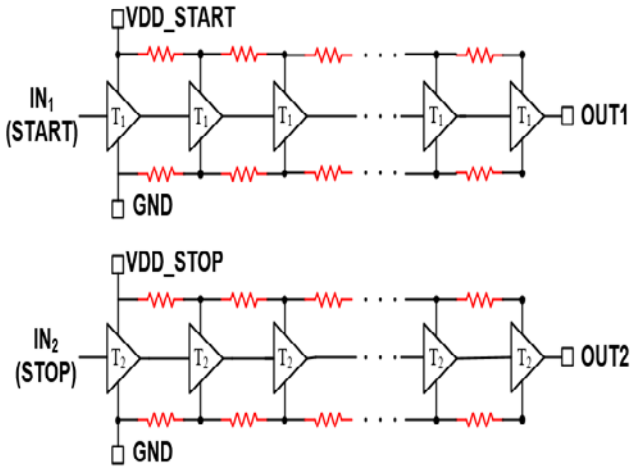


Fig.12. Schematic model with parasitic resistance

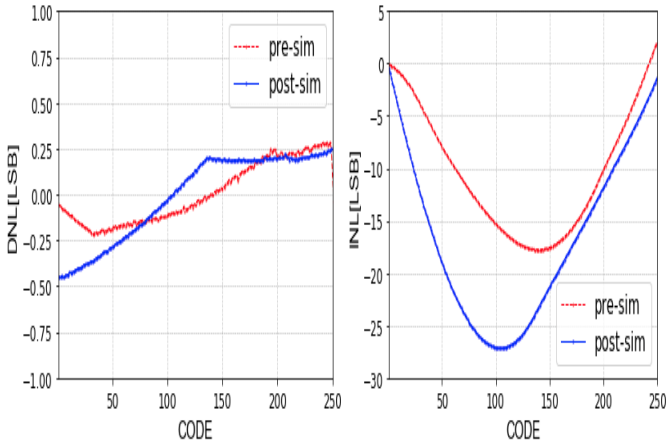


Fig.13. (a) DNL and (b) INL of pre-layout simulation with resistor modeling and post-layout simulation

D. Wire-bonding inductance simulation

The following is a description of the simulation that should be additionally verified for TDC design. We will examine the wire bonding simulation if the chip is bonded on a PCB board and the jitter simulation to determine the resolution of the TDC.

For reliable TDC operation, bonding wire simulation on the substrate can be considered as shown Fig.14. The inductance of bonding, which occurs when a chip is mounted on a PCB board, is assumed to be approximately 1nH/mm [8]. Voltage ringing occurs by bonding as shown in Fig.15, which causes delay imbalance and damages TDC linearity. The voltage ringing is proportional to the inductance and current. Therefore, the rebound is much greater if a lot of current flows like an amplifier stage with a large gain or delay buffer with sudden transition.

The voltage ringing between VDD and GND can be reduced by giving the same rebound through the on-chip capacitor. In determining the capacitance of the on-chip capacitor, enough capacitance is considered to prevent noise, including ringing. However, an appropriate capacitance should be checked to prevent resonance with bonding inductance.

To reduce the inductance component, the GND pin uses down bonding using the metal ground plane under the chip. VDD and GND are placed side-by-side because the mutual inductance component is canceled because the direction of the current at the VDD and GND pads is opposite.

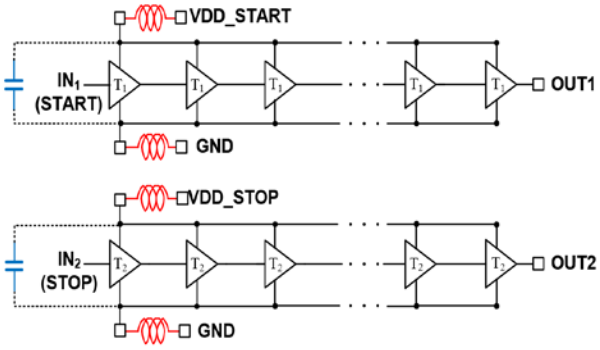


Fig.14. Schematic model with bonding wire inductance

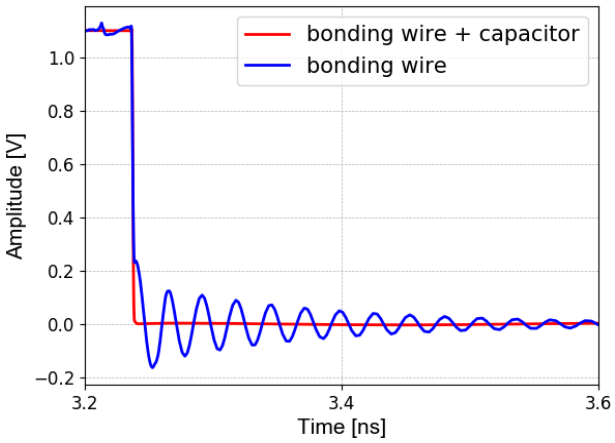


Fig.15. Ringing effect of bonding wire

E. Jitter and mismatch simulation

The causes of TDC nonlinearity are jitter and device mismatch. This variation can be seen from a global and local perspective. Global variations include process, supply voltage, and temperature, affecting overall TDC operation and producing offset or gain errors. Local variations include mismatch of threshold voltage, transconductance, and drain current, which leads to delay mismatch and directly affects DNL. These variations must be considered when determining the TDC time resolution, number of delays, and transistor size of the delay buffer [9,10].

The longer the length of the delay line, the larger the jitter. To guarantee integral error lower than 1 LSB error, the cumulative jitter of the entire delay line should be lower than the TDC time resolution. In other words, jitter limits the resolution of the TDC and the number of bits representing the TDC dynamic range.

Although there are many ways to measure jitter, the cycle-cycle jitter shows the difference between the period of the rising signal and previous period in Fig.16. Fig.17 shows the result of cycle-cycle jitter simulation in 200 cycles. The jitter of the 60th delay buffer is 1.7ps, and the 250th jitter is 3.5ps. If we observe more cycles, jitter distribution graph showing the Gaussian distribution. According to the simulation results, the TDC should aim at a time resolution of 3.5ps or more on 65nm 8bit TDC.

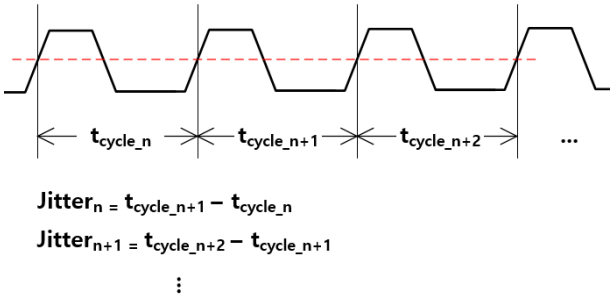


Fig.16. Concept of cycle-cycle jitter

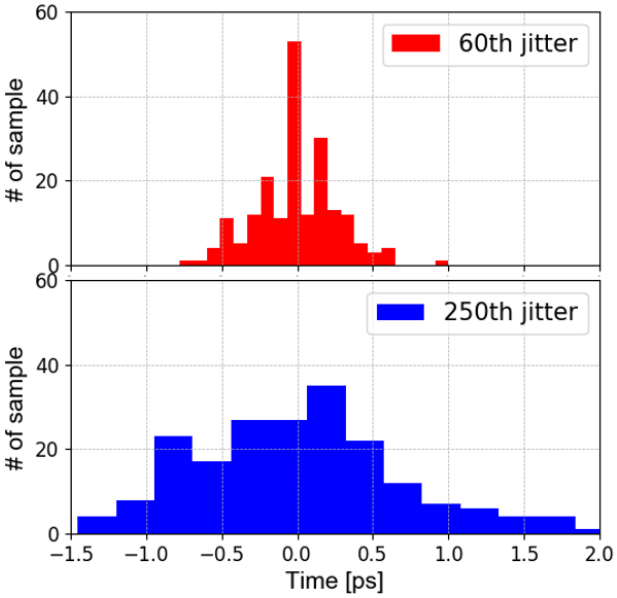


Fig.17 Cycle-cycle jitter distribution of 60th and 250th delay buffer

Fig.18 shows the result of a Monte-Carlo simulation with 200 samples showing the mismatch of the delay buffer. The average resolution of the delay buffer is about 16.2ps and has a standard deviation of 1.03ps. The 1.03ps mismatch variation is significantly lower than the TDC resolution of 18ps. The mismatch can be reduced if the L*W value is increased, however the power consumption increases accordingly. Considering this trade-off relationship, the size of the delay buffer can be determined according to the desired variation target [11].

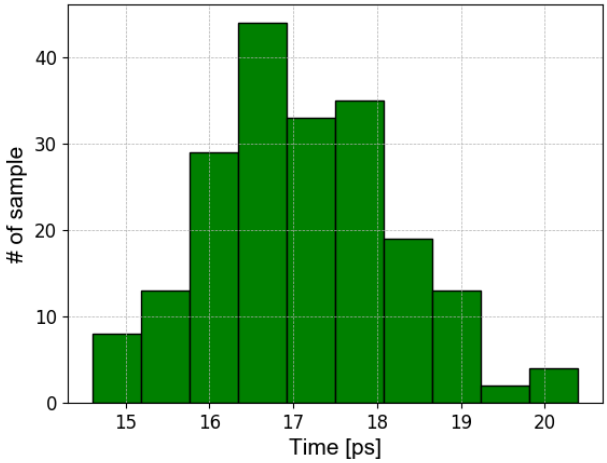


Fig.18. Delay buffer Monte-Carlo mismatch histogram

Most foundries provide a standard deviation of the threshold voltage or drain current mismatch according to the $\frac{1}{\sqrt{L \times W}}$ value with Monte-Carlo simulation. Circuit designer can refer to the results of these Monte Carlo simulations on the PDK to find the right transistor size for the desired standard deviation.

IV. CONCLUSION

The nonlinearity of the TDC measurement was analyzed from the viewpoint of layout, and the pre-layout simulation with the parasitic resistance modeling and the post-layout simulation were verified. We introduced jitter and monte carlo simulations that affect the nonlinearity of TDC, and we check the cycle-cycle jitter according to the number of delay and the delay buffer mismatch. The Cadence Virtuoso Specter and layout editor were used for simulation and layout, and the ADE XL for the monte carlo simulation.

This shows that there are many things to consider on the linear TDC operation, from setting TDC specification to the delay buffer and power line layout, including PCB board. By complementing the problems in this verification step, it is possible to improve the nonlinearity in the future TDC design and reduce the error of the bearing angle measurement. Low bearing angle error is expected to ensure accurate location information.

ACKNOWLEDGMENT

This work is supported by IDEC.

REFERENCES

[1] S. Gezici, Z. Tian, G. B. Giannakis, H. Kobayashi, A. F. Molisch, H. V. Poor, Z. Sahinoglu, "Localization via ultra-wideband radios: a look at positioning aspects for future sensor networks," *IEEE signal processing magazine.*, vol. 22, no. 4, pp. 70-84, July 2005.

[2] W. Gerok, M. E. Hadidy, S. A. E. Din, T. Kaiser, "Influence of the real UWB antennas on the AoA estimation based on the TDoA localization technique," *IEEE Middle East Conference on Antennas and Propagation (MECAP 2010)*, March 2011.

[3] B. G. Yu, G. H. Lee, H. G. Han, W. S. Ra and T. W. Kim, "A time-based angle-of-arrival sensor using CMOS IR-UWB transceivers," IEEE Sensors Journal., vol. 16, no. 14, pp. 5563-5571, July 2016.

[4] M. K. Kang and T. W. Kim, "CMOS IR-UWB Receiver for ± 9.7-mm Range Finding in a Multipath Environment," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 9, pp. 538-542, August 2012.

[5] Vossiek, M., Wiebking, L., Gulden, P., Wieghardt, J., Hoffmann, C., & Heide, P., "Wireless local positioning," *IEEE microwave magazine* pp. 77-86, 2003.

[6] P. Dudek, S. Szczepanski, J. V. Hatfield, "A high-resolution CMOS time-to-digital converter utilizing a Vernier delay line," *IEEE Journal of Solid-State Circuits.*, vol. 35, no. 2, pp. 240-247, Feb 2000.

[7] R. A. Hastings, *The art of analog layout*, New Jersey: Pearson Prentice Hall, 2006.

[8] B. Razavi, *Design of analog CMOS integrated circuits (International Edition)*, John Wiley & Sons, 2001.

[9] L. Vercesi, A. Liscidini, R. Castello, "Two-dimensions Vernier time-to-digital converter," *IEEE Journal of Solid-State Circuits.*, vol. 45, no. 8, pp. 1504-1512, August 2010.

[10] T. H. Jin, H. G. Han and T. W. Kim, "Time-of-Arrival Measurement Using Adaptive CMOS IR-UWB Range Finder with Scalable Resolution," *IEEE Transactions on Circuits and Systems I: Regular Papers.*, vol. 63, no. 10, pp. 1605-1615, September 2016.

[11] M. J. M. Pelgrom, A. C. J. Duinmaijer, A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE Journal of solid-state circuits.*, vol. 24, no. 5, pp. 1433-1439, October 1989.

Hyun Min Koh received the B.S. degree in electrical engineering from Yonsei University, Seoul, Korea, in 2017, and is currently pursuing M.S. degree at Yonsei University.

His current research interests include RF and mixed-signal IC and system.