Low Noise, Low Power 5-Channel Sonar Signal Conditioning Receiver with 1.5 MS/s - 12.5 MS/s 16-bit Sigma-Delta ADC for Ocean Acoustic Measurements

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***Abstract* - This paper presents a design of 5-channel receiver for ocean acoustic measurement in a very noisy environment. When measuring the distance in the ocean with the sonar signal, the input signal level to the receiver is drastically changed depending on the distance between the transmitter and objects. Thus, the receiver with low sensitivity and wide dynamic range is proposed in this work. In order to minimize the Input-Referred (IR) noise for low sensitivity of the receiver, low noise pre-amplifier is proposed and implemented achieving the noise of 29.6 nV/√Hz at 50 kHz. In addition, Sigma-Delta Analog-to-Digital Converter (SD ADC) with variable sampling rates is proposed by using clock splitting technique in the Sigma-Delta Modulator (SDM) core. Also, the decimation factor of the digital filter placed after the SDM in the SD ADC can be controlled to reduce the power consumption. Thanks to these techniques in the SD ADC, we can implement the reconfigurable sampling rates from 1.5 MS/s to 12.5 MS/s with low power consumption. In order to overcome the limitation of the number of pins for multi-channel application, Parallel-to-Serial (P2S) interface is proposed and designed in the receiver. The 5-channel receiver in this paper is implemented in 0.18μm CMOS process and die area is 14.44 mm2. The total power consumption of this chip is 46.8 mW under the supply voltage of 2.4 V. The measured sensitivity and dynamic range are -100 dBV and 100 dB, respectively. The measured SNDR at the output of the SD ADC is 82.02 dB when the input signal frequency and sampling frequency are 7 kHz and 6.25 Msps, respectively. The maximum phase error between 5 channels is measured to be ± 0.8 °.**

***Keywords*— Multi-channel, Receiver, Sonar sensor**

I. INTRODUCTION

Sonar system has been actively studied from various perspectives such as sensor modeling, signal processing of the ultrasonic signal. Also, the signal processing circuits such as Analog-to-Digital Converter (ADC) have been actively researched. [1-7] The recent trends are more focusing on the sensor array than a single sonar sensor. Sensor array can have advantages in terms of reducing area and lowering costs accordingly. [8-9] In order to process signal from sensor array, multi-channel receiver is essential. Figure 1 shows the ocean acoustic measurement environment. The environment has many noise sources and the receiver is exposed to those noise sources. Many noise sources in the ocean environment degrade the performance of the receiver. In Figure 1, the distance between Object1 and Receiving Equipment is larger than d2, distance between Object2 and Receiving equipment. Especially, when receiving signal from the farther object, noise sources reduce the SNR performance much more. Thus, this measurement environment shown in Figure 1 requires the receiver with the low noise and Input-Referred (IR) noise should be lowered to improve the Signal-to-Noise Ratio (SNR) and sensitivity of the receiver. On the other hand, as the distance between the object and Receiving equipment is closer, the input signal level of the receiver will be increased, which can cause the nonlinear harmonic distortion in the receiver. For processing small and large input signal level depending on the distance, high dynamic range and Automatic Gain Control (AGC) is necessary.

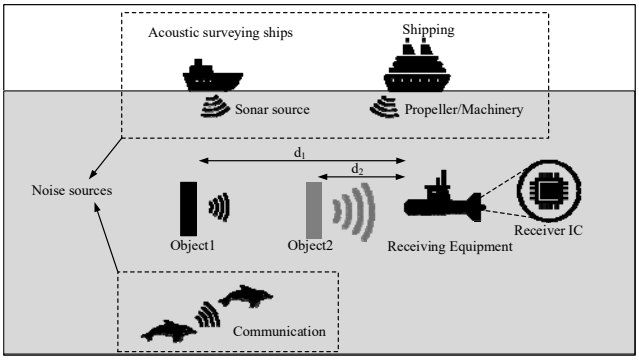

Figure 1. Environment of measuring distance on the ocean

In this paper, we propose receiver with the low noise pre-amplifier and wide dynamic range for sonar sensors. The pre-amplifier in the proposed receiver has the low IR noise of 29.6 nV / √Hz at 50 kHz. Also, it can apply the DC bias point of 1.2 V to the external sonar sensors since they do not have the DC bias voltage needed for proper MOSFET

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operation. A receiver takes the signal from each sensor of the sensor array and processes it in the single channel. For sensor array, the technique integrating separate multichannel circuits for signal processing is essential. The proposed receiver also includes the Sigma-Delta ADC (SD ADC) with reconfigurable decimation factor, and sampling frequency can be varied with oversampling ratio (OSR). In this paper, we propose and design 5-channel low noise receiver with SD ADC with reconfigurable sampling rate of 1.5 MS/s – 12.5 MS/s.

II. PROPOSED RECEIVER

The system specification of the proposed receiver is shown in Table 1. Input voltage amplitude range is from -100 dBV to -29 dBV. This large range requires the large dynamic gain range in the receiver. This system requires the IR noise less than -150 dBV / √Hz. When multiple input signals go to the proposed receiver in the same phase, the output of that is less than 1 degree. Parallel-to-Serial (P2S) is essential due to the number of channel. With P2S circuit, reducing the number of data output pins is available. Figure 2 shows the equivalent circuit of the unit sensor of the sensor array. Input signal is modeled as voltage source and sensor can be modeled with resistor and capacitor.

The block diagram of the proposed receiver is shown in Figure 3. Each channel of the proposed receiver consists of pre-amplifier, variable gain amplifier (VGA), band pass filter (BPF), SD ADC and P2S circuits into one chip. When differential signal comes from the sensor array, each signal goes into each channel of the 5-channel receiver IC.

TABLE I. System specification

Parameter	Specification
Input voltage amplitude(dBV)	-100 ~ -29
Supply voltage (V)	2.4
The number of Channel	5(in 3.8 mm * 3.8 mm size)
Dynamic range(dB)	20 ~ 100
Resolution(bit)	16
Sampling frequency (Hz)	> 2.5 M
IR Noise(dBV / √Hz)	< -150
Phase error between channels(degree)	< ± 1

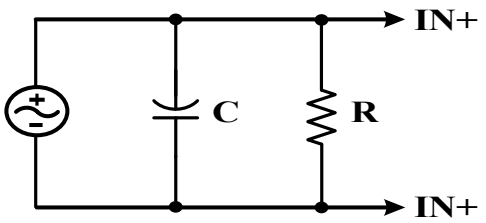


Figure 2. Equivalent circuit of sensor on the input

The receiver is designed to minimize the noise maximizing the SNR with the high resolution SD ADC. Each MOSFET in the pre-amplifier of input stage is designed to be large to reduce the flicker noise. Depending on input signal level, VGA can adjust its gain to make input signal level of the ADC to the Full Scale (FS). BPF has the function of DC offset cancellation and reducing noise at the high frequency. SD ADC is implemented to obtain high resolution for the low sensitivity sonar sensor application by applying variable oversampling and chopping scheme in the amplifier. In addition, Sigma-Delta Modulator (SDM) in the SD ADC uses clock splitting technique and adopts digital filter with adjustable decimation factor for reconfigurable sampling frequency. Parallel-to-Serial (P2S) interface is integrated for multichannel receiver due to the limitation of the pins. SPI Controller is designed to control gain of IC depending on the input signal level.

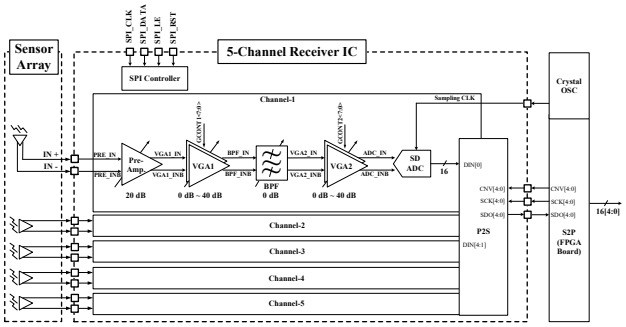


Figure 3. The block diagram of the proposed 5-Channel Receiver IC

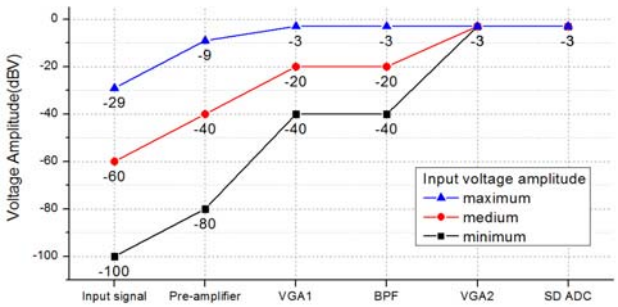


Figure 4. System budget of the proposed receiver with respect to input signal amplitude

III. PROPOSED RECEIVER

A. Pre-amplifier

Since the ocean measurement environment requires low noise receiver due to many noise sources around it, one of the most important issues is to increase the signal-to-noise ratio (SNR) in the high resolution receiver. In order to increase the SNR, lowering noise level of the input signal to ADC is necessary. In the receiver in this paper, the pre-amplifier is designed to lower the noise power for high SNR at the output of the ADC. In general, IR noise of the pre-amplifier dominantly determines noise performance of the whole receiver. Therefore, to design the receiver having low noise, it is important to minimize IR noise of the pre-amplifier. In addition, pre-amplifier plays the role to suppress noise from VGA1 and BPF by providing the gain of 20 dB. The schematic of pre-amplifier is shown in Figure 5. Since the input DC voltage level of the application is not determined by the external Sensor, we design the pre-amplifier for shifting the DC level to 1.2 V in order to meet the bias condition of VGA1. The size of input MOSFET is optimized so that input referred noise be minimized. With

this pre-amplifier, IR noise of the proposed receiver is simulated to be 29.6 nV / √Hz at 50 kHz.

Figure 6 shows the OP-Amp used in the pre-amplifier. Two-Stage Op-Amp with PMOS inputs is designed. Miller compensation with R and C is applied to guarantee the Phase Margin (PM) of 60 °. With the OP-Amp, the noise contribution of all the devices in the Op-Amp is analyzed as shown in Figure 7. In Figure 7, IR noise is lowered by optimizing MOSFET size and bias current. Before optimization, flicker noises of the input MOSFETs are dominant factor. Thus, we reduce their noise to almost 1/10 than those before optimization. Figure 8 presents the IR noise simulation result of the pre-amplifier showing the noise of 28 nV / √Hz at 50 kHz.

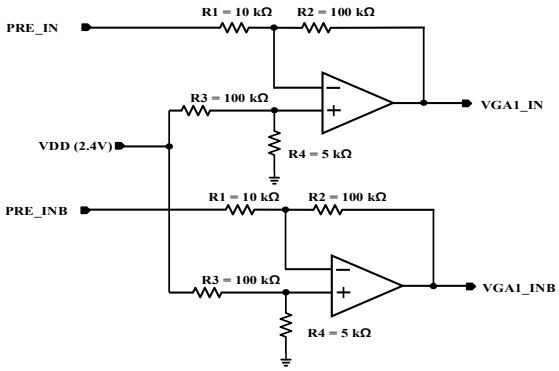


Figure 5. Schematic of pre-amplifier

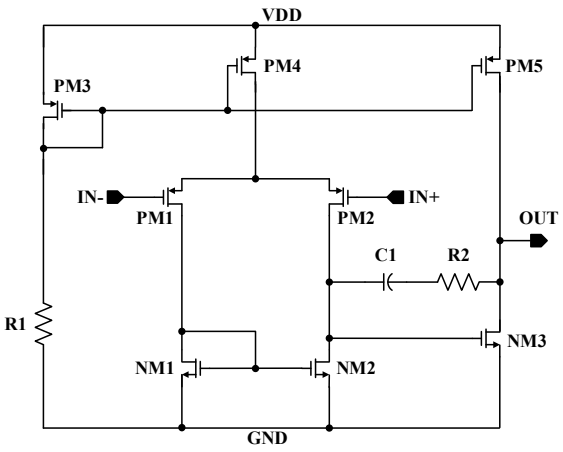


Figure 6. Schematic of OP-Amp in the pre-amplifier

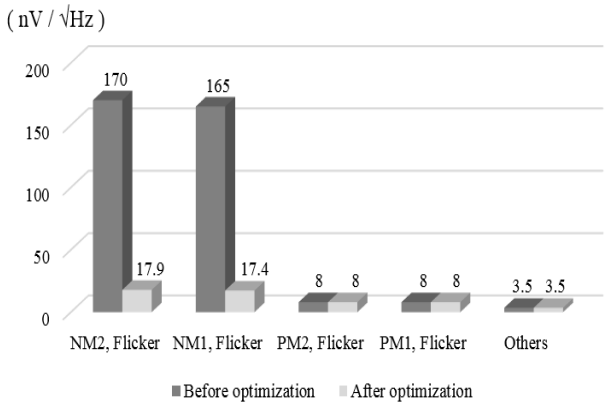


Figure 7. IR noise comparison before optimization and after optimization

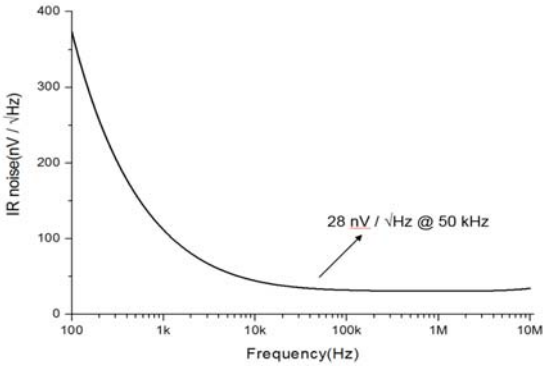


Figure 8. Noise simulation result of pre-amplifier

B. Variable Gain Amplifier

For high resolution of the SD ADC, precise gain control is needed. The proposed receiver has the function of controlling the gain with 1-dB step. As shown in Figure 2, input signal goes through the VGA1, BPF, and VGA2, sequentially. The maximum gains of VGA1 and VGA2 are 40 dB, respectively. Figure 9 shows the schematic of VGA1 and VGA2 uses exactly same structure as VGA1. Besides, they are designed to be adjustable using a resistive feedback structure by 1-dB step control depending on input signal level. As the signal amplitude is larger, lower gain is provided for meeting the input voltage range of SD ADC. AC simulation result of VGA1 is shown in Figure 10. Total gain is from 0 dB to 40 dB and it provides variable gain step of 1-dB.

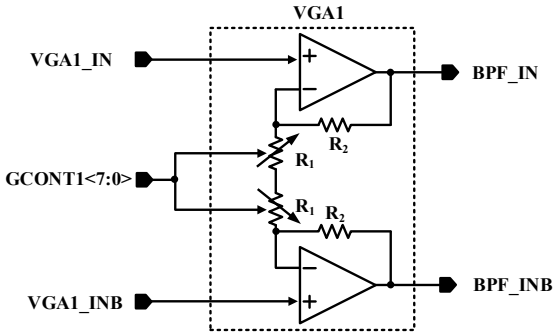


Figure 9. Schematic of VGA1

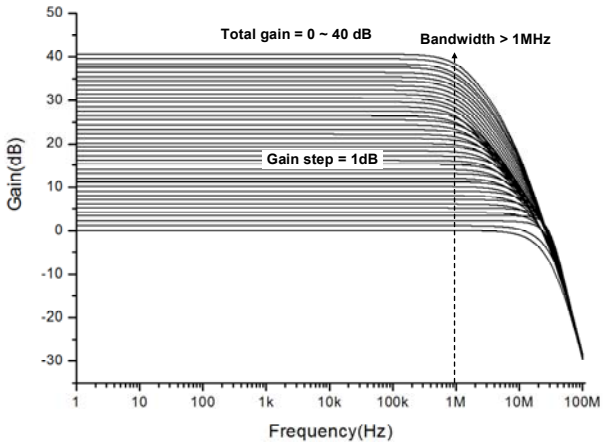


Figure 10. AC simulation result of VGA1

C. Band Pass Filter

For cancelling the dc offset and suppressing noise at high frequency, Active-RC Band-Pass Filter (BPF) is designed in the proposed receiver. The schematic of BPF is presented in Figure 11. BPF is designed as 4th order, Chebyshev type. In terms of noise performance, VGA1 is positioned right after pre-amplifier because the noise characteristic of BPF is worse than those of the VGA1 and VGA2. Thus, the noise from BPF can be attenuated by the gain of pre-amplifier and VGA1.

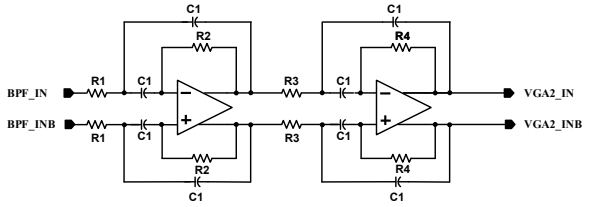


Figure 11. Schematic of Band-Pass Filter (BPF)

D. Sigma-Delta ADC

Figure 12 is the proposed simplified SD ADC designed in this work. SD ADC consists of SDM and digital filter. In this application, we designed high resolution for the ocean measurement environment. In order to reduce the noise, SDM is designed to push out the noise to higher frequency which can be filtered by the following digital filter. Decimation filter is designed to control the decimation factor to lower the current consumption.

Figure 13 shows the block diagram of SDM. The second order discrete type SDM with Cascaded Integrator Feed-Back (CIFB) structure is implemented. Two integrators and 1-bit Quantizer is used.

The schematic of the SDM is shown in Figure 14. The sampling operation is performed in the sampling capacitors as shown in the Figure 14. The differential signals (V_{IN} and V_{INB}) come from the analog circuits including pre-amplifier, VGA and BPF. Input differential range of SDM is 2 V_{pp} and common mode level is 1.2 V. In the first integrator, the coefficient value is determined by the ratio of the sampling capacitor (C_I/4) and integration capacitor (C_I).

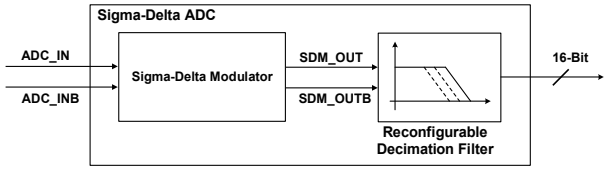


Figure 12. Simplified block diagram of the proposed SD ADC

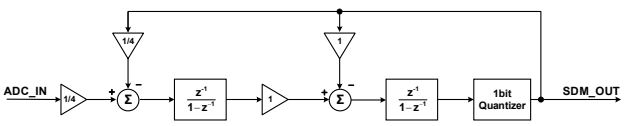


Figure 13. Block diagram of the Sigma-Delta Modulator(SDM)

Figure 15 shows the schematic of OP-Amp used in SDM shown in Figure 14. The amplifier has gain-boosted Folded-Cascode structure. In order to reduce the flicker noise at the

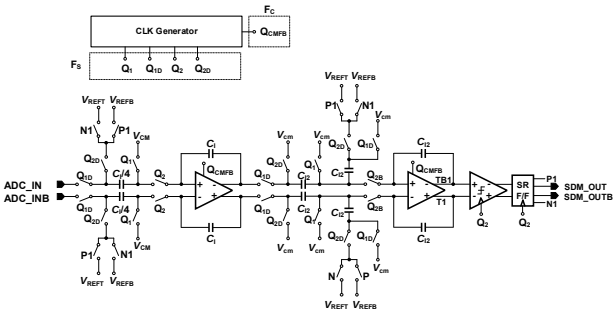


Figure 14. schematic of the designed Sigma-Delta Modulator(SDM)

low frequency, the chopping scheme is applied. The OP-Amp use the Chopper PMOS, Chopper NMOS, and Chopper_IN with their control switches. The chopper pushes out the noise in the signal band to higher frequency. The chopper circuits basically operate based on the clock. The clock is generated by CLK Generator shown in Figure 15. Besides, the common mode feedback (CMFB) circuit is designed to maintain the output common mode voltage level. Since in the high gain amplifier, the circuit that keeps the output bias voltage is essential. In order to use high sampling frequency, CMFB clock should be separated from sampling clock. If CMFB clock is same with sampling clock, the gain of OP-Amp used in the SDM is reduced. In that case, resolution of SD ADC is also degraded. In this paper, we split CMFB clock from the sampling clock.

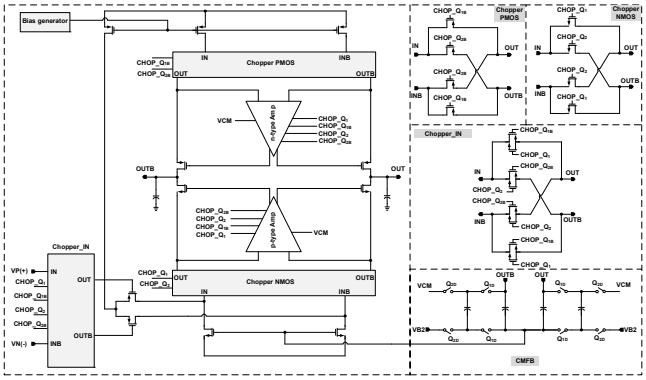


Figure 15. Schematic of OP-Amp in the proposed SDM

Figure 16 shows the schematic of the clock generator of the SDM. The circuit generates clock signals Q_1, Q_{1D}, Q_2, and Q_{2D}. Also, inverted signals, Q_{1B}, Q_{1DB}, Q_{2B}, and Q_{2DB} from Q_1, Q_{1D}, Q_2 and Q_{2D}, are also generated through clock generator circuit. Figure 17 shows the clock signal waveforms generated by the clock generator circuit. Since Q_{1B}, Q_{1DB}, Q_{2B}, and Q_{2DB} are inverted form of Q_1, Q_{1D}, Q_2, and Q_{2D} signals. Q_1 and Q_2 signals are non- overlapped clocks as well as Q_{1D} and Q_{2D} signals.

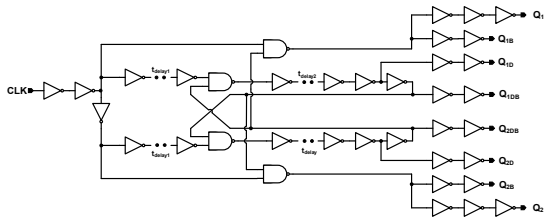


Figure 16. Structure of the non-overlap two-phase clock generator

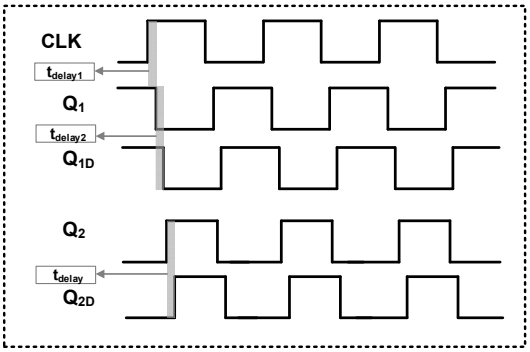


Figure 17. Clock signals generated by the clock generator block

Figure 18 shows the structure of the proposed comparator. Since the power consumption is smaller than that of the static type, a dynamic type of comparator is designed. The differential output of the second integrator is connected to the INP and INN inputs of the comparator. The outputs of the comparator (SDM_OUT and SDM_OUTB) are determined by latches. Q_1 and Q_2 clock signals control the comparator clocking and the P1 and N1 signals are determined to control some switches in the SDM as shown in Figure 14.

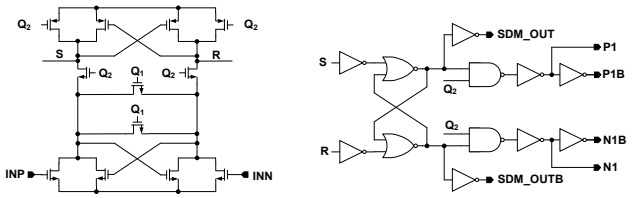


Figure 18. Structure of the comparator

The proposed SD ADC consists of mainly SDM and digital filter. A digital filter has a role as cutting the noise on the high frequency band. The main function of the SDM is pushing out the noise to higher frequency than input signal frequency. And the order of the SDM determine the slope of the output noise shaping. The higher order SDM makes the output noise shaping more sharp on the frequency domain. For applying digital filter to the high order SDM, the digital filter should have high power, large area with cascaded structure. In the conventional design, decimation factor of the digital filter is dependent value on the OSR of the SDM. In this paper, digital filter with controllable decimation factor and controller is presented.

The SDM in this paper has 2nd order configuration as it is shown in Figure 12. For small area, sinc3 type filter is adopted for the proposed receiver. The block diagram of the proposed decimation filter is shown in Figure 19. It includes the Integrators and Comb filters with cascaded structure. The controller is used to control decimation factor. Using the CONTROLLER block, the register width and proper clocking within the filter stages are selected. Integrator clock is same as sampling clock (Fs) of the SDM whereas Comb can be operated with sampling clock divided by decimation ratio (Fs/D). This process helps decimation filter to reduce the power dissipation at Comb stage of the CIC filter. This clock is controlled by the CONTROLLER block according to the requirements of the decimation ratio. Register size can be varied through the CONTROLLER when changing decimation ratio. This is because integration and differentiation (Comb) require different register sizes when the decimation ratio changes. Register sizes are proportional to the decimation ratio. They are related by the following equation (1)

$$\text{World Length} = L\,(\log_2 D \cdot M) + W_{in} \qquad (1)$$

In this Equation (1), L is the number of stages in CIC filter. D is decimation factor with variable features, M is the number of delays and W_{in} is the input word length. Inside the integrator and comb filter, register size is controlled for the specific decimation ratio. Output of the filter has the 14 Most Significant Bits (MSB) selected from single wide register (main register).

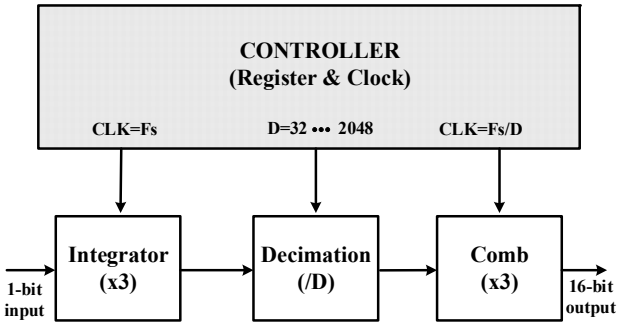


Figure 19. Proposed block diagram of the decimation filter

Figure 20 shows the CONTROLLER which is used in decimation filter. The CONTROLLER includes the Clock Controller and Register Controller. Clock Controller provides the clocks for needed in the Comb filter, Integrator, and CIC filter. Equation (1) presents how register size is calculated and maximum size for D=2048. This will be the main register used by all filters. The controller will select MSB 14-bits from this register based on the decimation factor and will discard the remaining bits.

Also, the controller operates by sampling clock sample with that used in SDM. The necessary clocks for the integrator, comb and other control blocks are generated based on this sampling clock. D_CNTRL (4 bits) is used to select among various options of the decimation factor (32, 64, ..., 2048). The register controller block selects 14 MSBs from the main register and assigns them to the output by dropping the LSB.

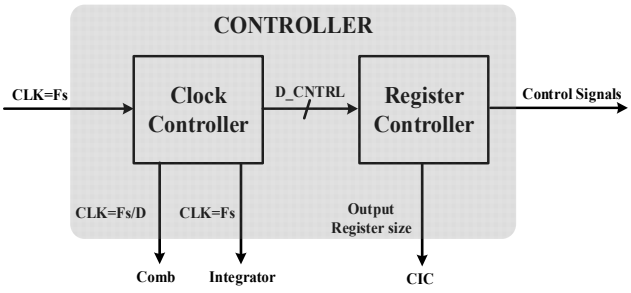


Figure 20. Proposed controller for configurable CIC filter

E. P2S-S2P Interface

The proposed receiver implemented the serial interface circuit inside the IC. For pin-constrained application, P2S interface is necessary to send the data. [10] Figure 21 shows the block diagram of the P2S-S2P used in the proposed receiver. SYNC is synchronization signal, DIN means parallel data input and SDO is serial data output. P2S interface is designed inside the IC and S2P is in the FPGA board. ADC output is the parallel data, then the data goes to P2S interface and its output is serial form data. This P2S-S2P interface has two synchronization modes which are high throughput mode (HTM) and highly synchronized mode (HSM).

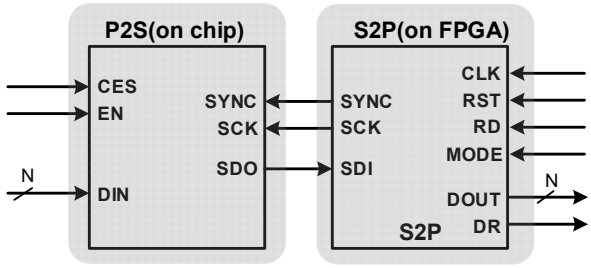
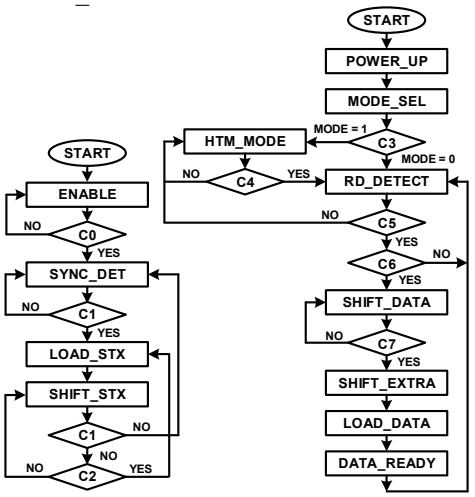


Figure 21. P2S and S2P block diagram

In HTM, SYNC is pulled down and MODE signal is high. After that, P2S receives data from DIN and at the active edge of clock SCK, transmits it to SDO. SDO is transmitted in serial from MSB to LSB. In this mode, no overhead bits or extra clock cycles exist. At the time that the communication between P2S and S2P interface starts, P2S and S2P are synchronized at the negative edge of SYNC once. Firstly, MODE is pulled down and the mode HSM that P2S and S2P synchronize is enabled after all serial data is sent and received. Only when RD is high, P2S takes sample and transmits it to P2S. This mode is determined due to features of the proposed receiver which does not need continuous data. For the high performance P2S interface operation, f_{sck} (the serial clock frequency) is necessary. It is given in Equation (2).

$$f_{SCK} \geq F_{ADC} \times N \qquad (2)$$

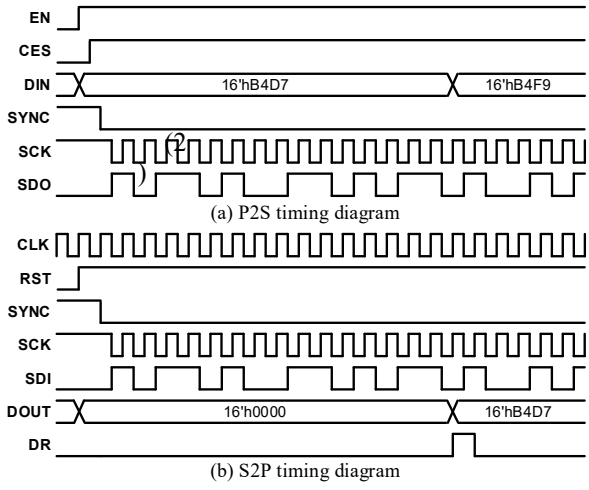
In the Equation (2), N is the resolution and F_{ADC} is the sampling frequency of ADC, respectively. The P2S and S2P interface is synchronous finite state machine (FSM) model based design. Figure 22 shows the FSM flow chart for P2S and S2P. Timing diagram of each data is presented in Figure 23. The P2S circuit in this paper is enabled only when EN from control logic is pulled high. For P2S, the positive or negative active edges can be selected by clock edge select signal (CES). On POWER_UP stage, P2S controller moves to ENABLE. Then, the controller goes to SYNC_DET state and hold on for SYNC negative edge. When SYNC is released from S2P, the P2S controller jumps to the next stage, LOAD_STX. In LOAD_STX state, the parallel data DIN is loaded from the internal register transmitting the MSB to SDO. Then, in SHIFT_STX state, if SYNC is held low, the internal register value is shifted one bit to the left and the MSB of the register is transferred to the SDO pin remaining for N-1 SCK clock cycles. In case of HTM enabled, the controller moves state to LOAD_STX for taking SD ADC sample. The controller goes back to LOAD_STX state for receiving next ADC sample. Or, it jumps back to SYNC_DET for resynchronization in case of HSM. The FSM for S2P controller is presented in Fig. 15(b). Data stays in POWER_UP state after reset for one clock cycle. Then it goes to MODE_SEL state and MODE signal from control logic select the mode HTM or HSM. When MODE is asserted, HSM is enabled and the controller get direction to HTM_MODE state.



(a) P2S FSM (b) S2P FSM

Figure 22. Serial interface FSM diagram

In this state, SYNC is pulled low for synchronization between S2P and P2S. Also, S2P enables the SCLK clock and starts to receive serial data at SDI from S2P. The bits are shifted in serial inside the internal register. There is a counter for checking the number of bits received from P2S.



(a) P2S timing diagram

(b) S2P timing diagram

Figure 23. Serial interface timing diagram

If N bits are received, N-bit DOUT load the register bits. Additionally, in order to announce the reception of the data to control logic, RD is changed to pulled high for one clock. In case that MODE is deasserted to select HSM during HTM, the controller goes to RF_DETECT state after processing the

data. When HSM is enabled, the controller moves to SHIFT_DATA state after waiting the assertion of RD on RD_DETECT state. SYNC is pulled down and it happens to shift serial data to an internal register on all rising edges of CLK. This is the process to receive N-1 bits. After that when SYNC is pulled up in SHIFT_EXTRA state, another shift is performed. In LOAD_DATA state, N-bits on internal register goes to DOUT. When state changes to RD_DETECT state, there is announcement for data ready. In RD_DETECT state, controller senses the RD signal after checking the mode switch condition. After synchronization, with continuous high RD, HSM-CR of the S2P stay same state to enable RD in HSMSR sub-mode or launch to receive the serial stream.

IV. EXPERIMENTAL RESULTS

Figure 24 is the chip photograph of the proposed receiver. Total area of the proposed receiver is 3.8 mm x 3.8 mm. It includes 5-channel with P2S interface. Figure 25 is the evaluation board for the proposed receiver. The evaluation board has the low noise low-dropout regulator (LDO) and Connector to Labview system. It uses SMA connector to receive the signal. Figure 26 shows the measurement environment of the proposed receiver. For measurement, the sine wave signal is applied by function generator. FPGA board has the function of S2P interface for testing P2S inside the IC.

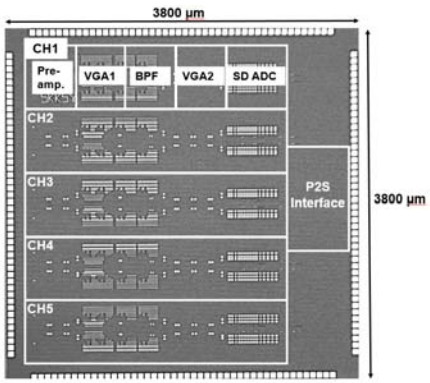


Figure 24. Chip photograph of the proposed receiver

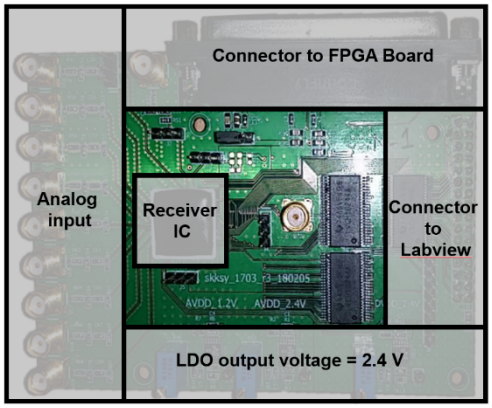


Figure 25. Evaluation board for the receiver IC

Figure 27 shows the AC simulation result including pre-amplifier, VGA1, VGA2, BPF. It has dynamic range from 20 dB to 100 dB. It shows the IR noise simulation result is around –150 dBV / √Hz. Table 2 shows the simulation result of SD ADC according to increasing sampling clock. Fs is sampling clock and Fc is the CMFB clock shown in Figure 14. If Fc is divided by Fs like this work, resolution is better especially when sampling clock frequency goes higher. [10]

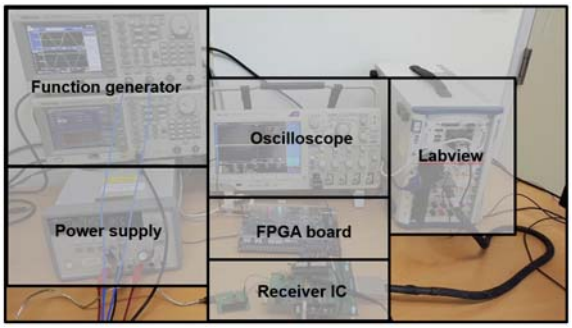


Figure 26. Measurement environment of the proposed receiver

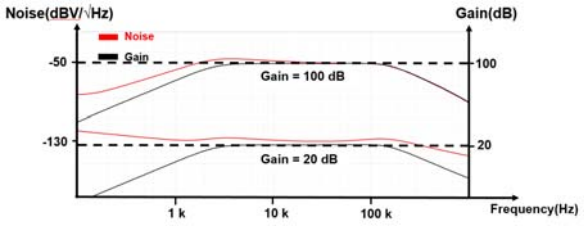


Figure 27. Noise simulation result with minimum gain and maximum gain

Table II. Simulation results of SD ADC

F_S(Hz)	OSR	Conventional structure		Proposed Structure	
		$F_C = F_S$		$F_C = F_S/16$	
		SNDR (dB)	ENOB (bits)	SNDR (dB)	ENOB (bits)
390.5 k	32	86.03	14.29	85.66	14.23
780 k	64	26.27	14.33	87.41	14.52
1.56 M	128	93.49	15.53	94.15	15.64
3.125 M	256	94.51	15.7	94.27	15.66
6.25 M	512	89.52	14.87	94.03	15.62
12.5 M	1024	74.35	12.35	92.59	15.38

The measurement result of BPF AC response is presented in Figure 28. It is flat at the frequency from 3 kHz to 130 kHz. Table 3 shows the noise measurement result of the proposed receiver. It shows the -150.36 dBV / √Hz according to adjusting gain. IR noise is output noise divided by gain. When signal goes to the receiver, the PSD result of the receiver is shown in Figure 29. It is normalized in the X axis to $F_{in}/(F_s/OSR)$. The PSD result is presented as decibels relative to full scale (DBFS) units. The SNR at the

fundamental frequency is 93.5 dB and 82.02 dB signal-to-noise and distortion ratio (SNDR). Figure 30 shows the phase difference measurement result between two channel when receiving 3 kHz signal.

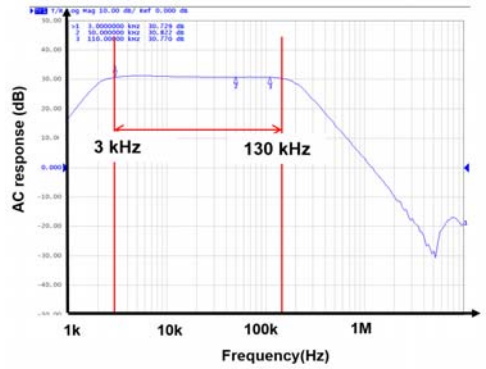


Figure 28. AC response of the band pass filter

TABLE III. Noise measurement result

Gain setting(dB)	Noise output (dBV / √Hz)
20	-126.35
29	-122.87
38	-115.6
47	-105.4
56	-92.38
65	-84.58
IR Noise (average) = -150.36	

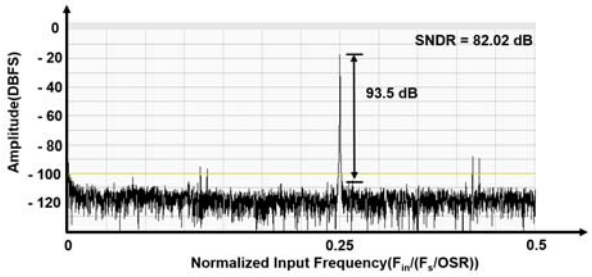


Figure 29. PSD measurement result of the proposed receiver with sinewave input

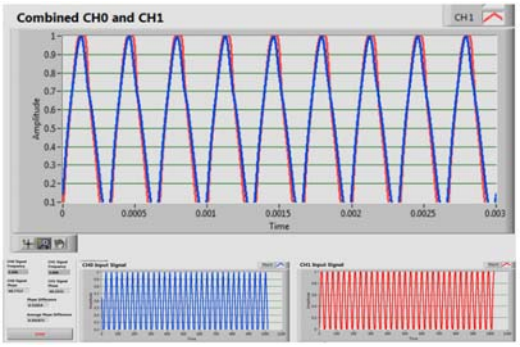


Figure 30. Phase difference measurement result between two channel

Table 4 shows the performance summary of the proposed receiver. The dynamic range is higher than those presented in [13]. The noise performance is better than that of [12]. Bandwidth of the input signal is higher than those of [11,12,13]. Since this work implemented reconfigurable structure of SD ADC, it can use variable sampling frequency that differs from [11,12,13]. Also, it can use higher sampling clock frequency than [11,12,13].

Table IV. Performance of the analog front-end

	This Work	**[11]**	**[12]**	**[13]**
Process (nm)	180	130	130	65
The number of channel	5	64	96	4
Dynamic range(dB)	20 - 100	N/A	N/A	40
IR Noise (nV/√Hz)	29.6 @ 50 kHz	N/A	2200 @ 10 kHz	N/A
Bandwidth (Hz)	2.8k - 130 k	1 k	< 10 k	25 k
Sampling frequency (Hz)	1.5 M – 12.5 M	N/A	31.25 k	10 M
Structure of ADC	Reconf igurable	Fixed	Fixed	Fixed
Supply voltage (V)	2.4	0.9 – 1.2	1.2	1.5
SNR (dB)	93.5	N/A	N/A	84.2
Phase difference (degree)	< ±0.8	N/A	N/A	N/A
Power consumption	46.8 m	1.8 u	6.5 m	68 u / 1-ch.
Area(mm^2)	14.44	6	25	0.03

V. CONCLUSIONS

In this paper, we propose a low-noise 5-channel receiver for receiving dynamic amplitude signal especially for low frequency system for ocean acoustic measurement environment. Since environment has noise sources, we design the proposed receiver with low noise performance. Furthermore, the power consumption the receiver in the ocean environment should be lowered due to portability. This proposed receiver is applied several design techniques including chopping architecture in SD ADC. And, SDM in the SD ADC is designed with clock splitting technique. Also, digital filter in the SD ADC is designed with controller to lower the power consumption.

The designed receiver has an input-referred noise of 29.6 nV / √Hz at 50 kHz and a total gain of 100 dB. The gain of the receiver is controlled with 1-dB step precise gain so that it can be changed according to the power variation of the input signal. It implemented SD ADC with reconfigurable structure and obtain 93.5 dB SNR performance. The receiver of this paper is designed with CMOS 0.18 μm and the chip area is 3.8 mm x 3.8 mm. Power consumption is 46.8 mW at 2.4 V supply voltage. The proposed receiver can be used in the very noisy environment especially ocean acoustic measurement.

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