A 10-Gb/s programmable and flexible transceiver with a FPGA

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***Abstract* – Digital design automation software tools have been very successful in achieving performance gains over the past 50 years as system IC density continues to increase. As the design of these mixed signal systems increases, the simulation time for verifying new algorithms becomes a significant part of overall system development time. However, it cannot be accurately verified using existing verification tools. In this thesis, we propose a programmable and flexible 10Gb/s transceiver that is a structure in which all the analog blocks that can be reused are implemented in the IC and the digital blocks that have always been a problem due to the difficulty of verification are implemented in the FPGA as a verification tool of mixed signal systems.**

I. INTRODUCTION

Most modern high-speed serial links are designed with analog blocks and synthesized digital blocks. In other words, mixed-signal system design is dominant. The main reason for the mixed system design is that the digital control block is designed and synthesized using VHDL language, which makes it much easier to design a complex digital system than to design it using full-custom. Based on these advantages, various digital functions are integrated in the IC to control the entire system. Examples of synthesized digital blocks include digital loop filters, controllers, and calibrators.

However, as the design of mixed-signal systems are caused by the system level functionality offered by synthesized digital blocks.

Most of operational issues of mixed signal systems are caused by the system level functionality offered by synthesized digital blocks. If there is a problem in the system level functionality of synthesized digital blocks caused by the lack of verification, the entire system often behaves erroneously. On the other hand, analog blocks can only be reused without major problems by adjusting only small tweaks of existing blocks most of the time.

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These problems are caused by the limitation of the method of verifying mixed-signal systems. Currently, there is no system-level simulation methods that can accurately and quickly verify mixed-signal systems. The actual operation of the chip is done in seconds, because we can only test micro seconds using existing simulation tools.

Therefore, most of them are verified using only matlab or verilog level simulation, so the BER can only be confirmed at the level of $1e^{-6}$, which is an uncertain verification method. For these reasons, there are problems with various functionality issues in the operation of the actual chip.

To solve these problems, the proposed solution is a design of a programmable and flexible transceiver. The mixed signal system consists of a few analog blocks and synthesized complex digital blocks.

II. EXPERIMENTS

A. System Architecture

The overall structure and operation of a circuit design is shown in Fig. 1. Basically, the circuit design is implemented in the analog blocks required for the High speed serial link, that is, the basic TRX for the transmission and reception of 10Gb/s data. In the FPGA, there are synthesized digital blocks, which can control basic analog TRX blocks using the data coming from the chip.

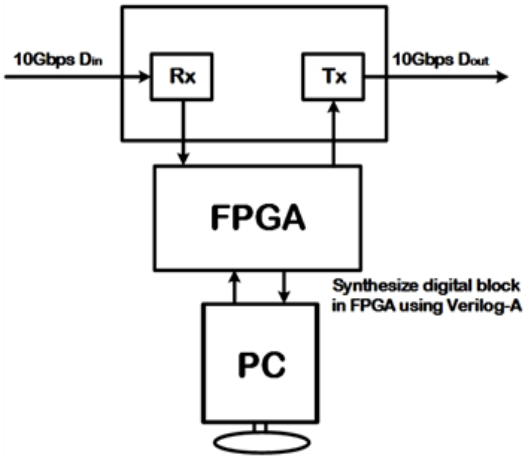

Fig. 1. Example of a chip-FPGA communication

As a result, the high speed serial transmission is executed through the connection of the chip and the FPGA. A 10Gb/s data is sampling, retiming, demuxing in the chip and enters the FPGA.

The FPGA sends out a signal to control the internal blocks of the chip using the received data. Then, the data is sent back to the TX of a chip from a FPGA, and the TX of a chip is muxing them to transmit serial data to 10Gb/s. As a result, the high speed serial transmission is executed through the connection of the chip and the FPGA.

B. Transceiver Architecture

The proposed transceiver as shown in Fig. 2 is configured through a connection between the proposed IC(LEGO chip) and the FPGA. The proposed IC implements basic analog blocks for operation as a 10Gb/s transceiver. Each block of the proposed IC transmits necessary information to the FPGA to implement various digital functions.

In addition, the proposed IC can be a stand-alone 10Gb/s transceiver. The proposed IC has receiver, transmitter, clock generator and digital blocks needed to form a closed loop within the IC, enabling it to operate as a stand-alone 10Gb/s transceiver.

In the FPGA, any digital functions can be implemented based on the information provided by the proposed IC.

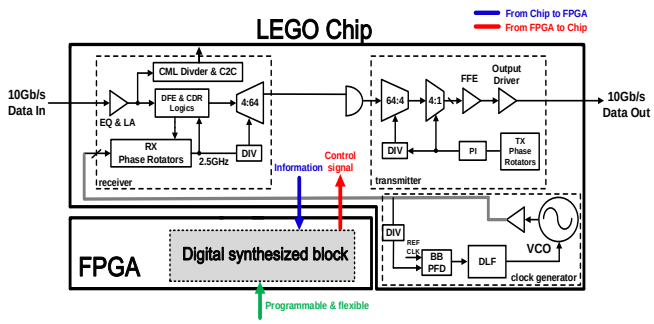

Fig. 2. Top Architecture of the transceiver.

C. Receiver Architecture

The receiver consists of analog blocks for generation information to send to the FPGA. Fig. 3 shows the block diagram of a 10Gb/s RX, which consists of a continuous-time linear equalizer(CTLE), a limiting amplifier(LA), CML divider and CMOS divider for SRCG, CMOS quadrate samplers with a one-tap loop-unrolled decision feedback equalizer(DFE), a retime, a 4:64 de-multiplexer(DEMUX), a synthesized CDR logic block for making a closed loop within the IC, and a phase-rotator-based multiphase clock generator(CML divider, Harmonic Rejection Poly Phase filter, Phase rotator, Phase interpolator(PI)).

The CTLE and LA recover the data damaged by channel loss. CMOS quadrate samplers with a one-tap loop-unrolled decision feedback equalizer sample 10Gb/s data. The DEMUX and re-timer convert 10Gb/s serial data into 156.25MHz parallel data to meet the maximum operating speed in the FPGA. The phase rotator adjusts the phase of multiphase clocks and samples the data.

As the result, as shown in Fig. 4, the receiver transmits various information generated by analog blocks such as de-multiplexed data and edge, divided data for SRCG, and the system clock for the operation of digital functions in the FPGA, which is processed by the FPGA and used to implement various digital functions.

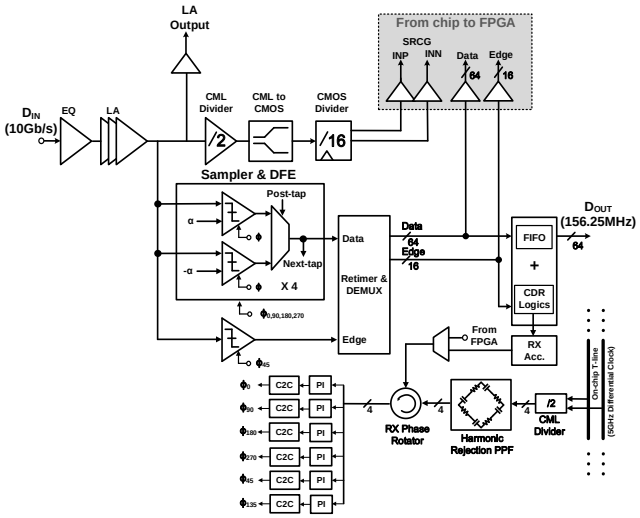

Fig. 3. The Architecture of the receiver.

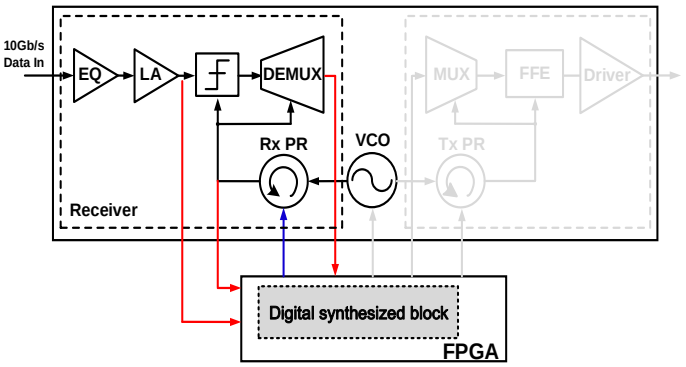

Fig. 4. The Overview of the communication between the receiver and the FPGA.

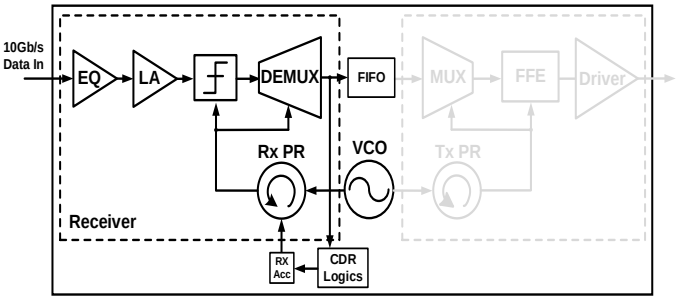

Fig. 5. The synthesized digital block in the receiver.

As shown in Fig. 5, simple digital blocks(CDR logics block) are synthesized in the receiver to form a closed loop in the IC and to operate as a stand-alone 10Gbps transceiver. A CDR logic and accumulator based on a Nyquist rate BBPD are used for phase lock and A FIFO transmits the parallel data to the transmitter in the IC.

D. Transmitter Architecture

The transmitter transmits 10Gb/s data by serializing 64 parallel data processed at the FPGA. Fig. 6 is the block diagram of the 10Gb/s TX. The TX consists of a 64:4 MUX implemented in static CMOS logic gates followed by a tap generator, and parallel 4:1 MUXs.

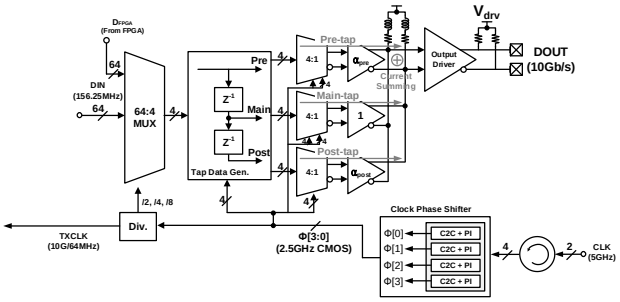

Fig. 6. The Architecture of the transmitter.

The FIFO in the FPGA receives 64 parallel data from the receiver and transfers it to the transmitter. TX eliminates the pre-cursor ISI of data through pre-emphasis and serializes it to transmit the 10Gb/s data. That is, it acts as a transceiver through the receiver-FPGA-transmitter.

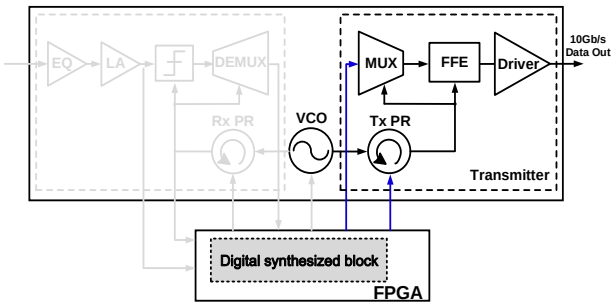

Fig. 7. The overview of the communication between the transmitter and the FPGA.

E. FIFO Architecture

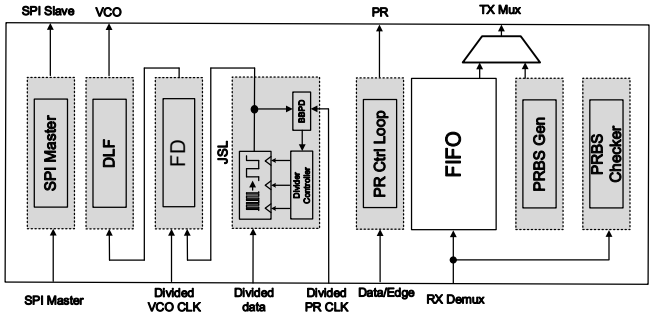

Fig. 8. The Architecture of the FIFO.

Fig. 8 is the block diagram of the FIFO. Any digital functions can be implemented in the FPGA. Each function is implemented by receiving the necessary information from the IC to implement it. For example, FPGA has digital blocks that control internal analog blocks in the IC, such as a phase rotator controller, Digital loop filter to control VCO, and Jitter-suppression loop for SRCG. Alternatively, digital functions for testing the performance of IC, like PRBS Generator/Checker, PRBS-based random generator can be implemented in the FPGA.

Basically, each digital function in the FPGA should serve to transmit control signals to the IC after they are processed data form the IC.

F. Examples of the digital functions in the FPGA

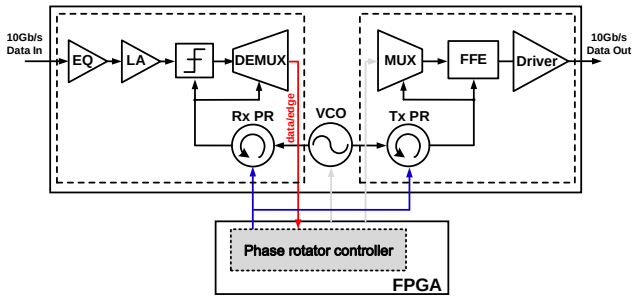

Fig. 9. Implementation of the phase rotator controller.

Fig. 9 shows the implementation of the phase rotator controller. The controller of phase rotators in the IC is implemented in the FPGA. The implementation process is as follows.

The de-multiplexed data and edge samples enter the phase rotator controller of the FPGA from the receiver of the proposed IC. They are provided to the CDR logic in the controller of the FPGA to accomplish single-edge-sensitive bang-bang phase detection. Then, control signals are generated by controlling the phase of phase rotators in the digital domain through accumulation and truncation. Consequently, control signals are transmitted from the FPGA to the IC to control phase rotators. That is, the loop bandwidth of the receiver and transceiver can be adjusted in the digital domain through the phase rotator controller in the FPGA.

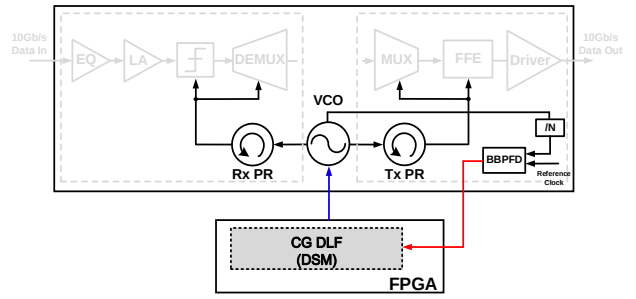

Fig. 10. Implementation of the digital loop filter in the Clock Generator.

Fig. 10 shows the implementation of the digital loop filter (DLF) for adjusting the frequency of the VCO. The CG DLF is composed of digital low-pass filter with adder, accumulator and dithering algorithm. The implementation process is as follows.

The frequency difference between the reference clock and the VCO clock is entered into the DLF in the FPGA through BBPFD in the clock generator of the IC. The accumulator in the DLF continues to accumulate frequency errors, of which 6 MSBs are used to coarse tuning the VCO frequency. Fine

tuning signals are composed of binary and thermometer codes to reduce the silicon area while minimizing the switching glitch.

Control bits in the DLF, which cannot be changed through a simulation, can be changed freely in the DLF implemented by the FPGA. Therefore, it is possible to check in real time how the frequency of VCO is adjusted accordingly.

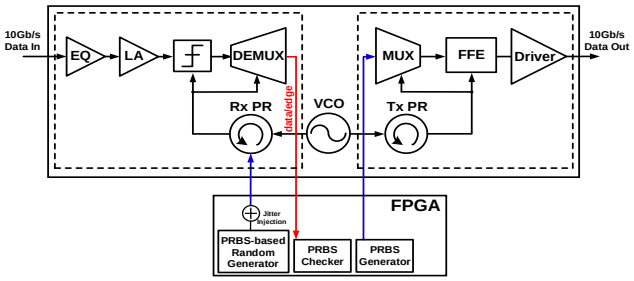

Fig. 11. Implementation of the Jitter tolerance self-test.

Fig. 11 shows the implementation of jitter tolerance (JTOL) self-test. JTOL self-test is possible by implementing PRBS Generator, checker, and PRBS-based random generator in the FPGA. The implementation process is as follows.

The transmitter in the IC sends jitter-free 10Gb/s data to the receiver in the IC through the PRBS Generator in the FPGA. A PRBS-based random generator in the FPGA injects jitter into the phase in the receiver of the IC. The phase rotator in the receiver tries to filter out the injected accumulation jitter and align the output clock signal with the jitter-free transceiver output data. Then, The output clock of the RX phase rotator samples the data and sends it to the PRBS Checker in the FPGA to verify BER. Consequently, we can measure JTOL of the IC by adjusting the amount of jitter injected from the PRBS -based random generator in the FPGA.

It is possible to verify the performance of the IC accurately and quickly by implementing the JTOL self-test in the FPGA that can hardly be verified in the simulation due to take too long.

G. FPGA Interface

The maximum speed that can be operated within the FPGA must also be considered to implement various digital functions in the FPGA. In order to determine the maximum clock speed of the digital function to be implemented in the FPGA according to the maximum operating speed of the FPGA, a simulation tool of the FPGA, STRATIX V was used for testing.

The maximum operating speed of the FPGA was 177.4MHz as a result of checking with the phase rotator controller which has the longest cycle among control schemes used in our lab. Fig 20 is the result of the test.

Based on result shown in Fig. 12, the speed of the system clock(156.26MHz) to be sent to the FPGA inside the IC and the speed of the de-multiplexed data (10G/64, 156.25MHz) were determined to ensure accurate design.

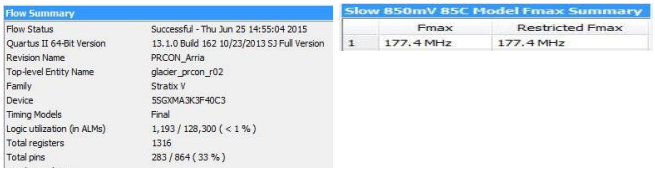

Fig. 12. The result of the test for determining the maximum operating speed in digital functions.

III. RESULTS AND DISCUSSION

A. Simulation setup

The proposed transceiver operates by communicating with the IC and the FPGA. Fig. 13 is a simulation setup to verify exact communication between the IC and the FPGA through the LVDS interface.

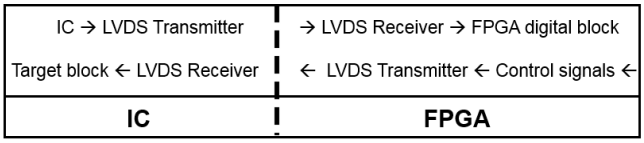

Fig. 13. Simulation setup.

The first step is to verify that the information is sent to the FPGA through the LVDS transmitter of the IC, and that the information is forwarded to the synthesized digital block exactly through the LVDS receiver of the FPGA.

The second step is to verify that control signals generated by the synthesized digital block are forwarded to the IC through the LVDS transmitter of the FPGA, and that control signals accurately control the target block in the IC through the LVDS receiver.

As a result, simulations were performed to verify that various digital functions implemented between the FPGA and IC were correctly operated through the LVDS interface.

B. System verification

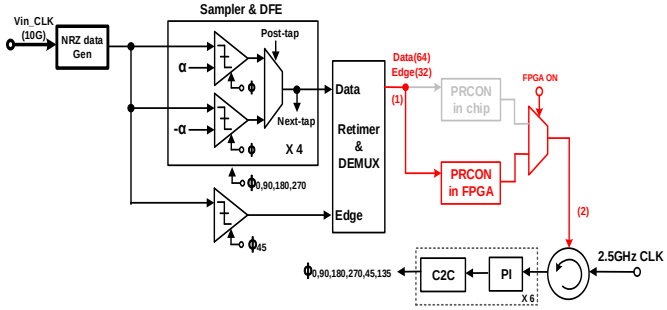

Fig. 14. The simulation for phase lock.

Fig. 14 shows the result of a simple simulation to verify the proposed system. I implemented the phase rotator controller in the FPGA and confirmed that the phase lock of the proposed transceiver is correct.

In order to meet the actual operating environment, the setup is as follows. De-multiplexed data/edge samples in the IC are transmitted to the FGPA through the LVDS transmitter, and then, the LVDS receiver of the FPGA receives these data/edge samples and controls the phase rotator through the phase rotator controller.

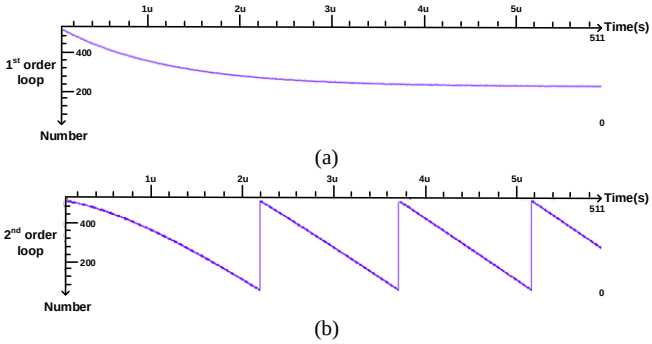

Fig. 15. (a) 1st order loop coefficient. (b) 2nd order coefficient.

Fig. 15 shows the result of the phase lock simulation. It can be seen that a coefficient of the 1st order loop converges to a specific value by phase lock between the FPGA and the IC as shown in the Fig. 15 (a).

In addition, even if there is a frequency offset, the frequency offset is removed by the 2nd order loop as shown in the Fig. 15 (b), so phase lock can be confirmed.

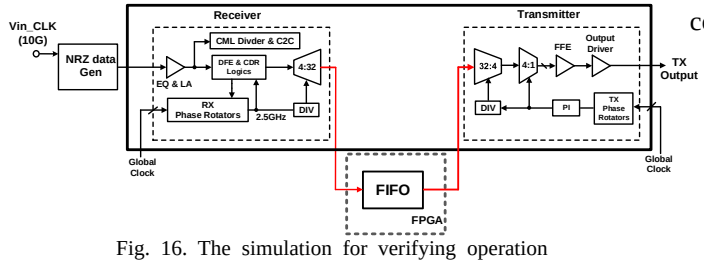

Fig. 16. The simulation for verifying operation of the proposed transceiver.

Fig. 16 shows another result of a simple simulation to verify the proposed system. This is a simulation process to verify that the proposed transceiver with the combined IC and FPGA operates correctly.

It is simulated to verify that the 10Gb/s NRZ data coming into the IC is transmitted correctly through the receiver of the IC, the FIFO of the FPGA, and the transmitter of the IC.

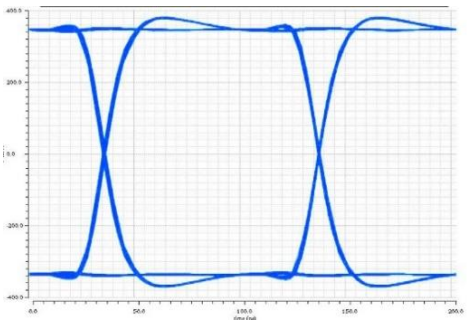

Fig. 17. The output eye diagram of the TX output.

Fig. 17 is the eye diagram measured by the simulation. It was simulated at TT, 27 degrees, 1V corner. The eye diagram shows that the voltage swing is 678mV and the deterministic jitter is 2.1ps, which means that that the data is transmitted accurately with very little noise through the proposed transceiver.

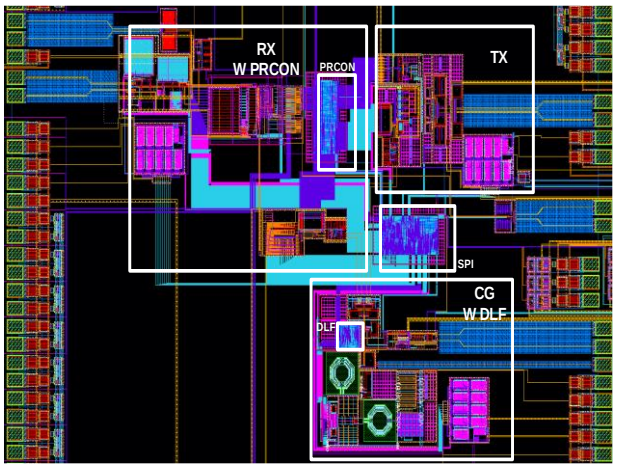

Fig. 18. The output eye diagram of the TX output.

Fig. 18 is the layout of the proposed transceiver. It was designed with a 65nm process and used a 1V supply voltage.

The proposed transceiver includes one TRX lane targeting 10Gb/s data rate. As shown in the Fig. 18, a total of 336 LVDS I/Os were placed in two rows on the edge of the IC to communicate with the FPGA.

TABLE I.
Power consumption of the full chip.

Technology		65nm CMOS
Supply voltage		1V
Data rate		10Gb/s
Power consumption (Receiver)	AFE(Linear EQ + LA)	48.91mW
	Datapath(Sampler + DFE + DEMUX)	12.78mW
	Clockpath(CML div + PR + 9PI)	9.94mW
Power consumption (Transmitter)	64:4 MUX	1.49mW
	Current summer(FFE)	19.63mW
	Out-driver (50ohm driver)	14.1mW
Power consumption (Clock Generator)	VCO	9.7mW
	VCO buffer	7.8mW
Total power		124.35mW

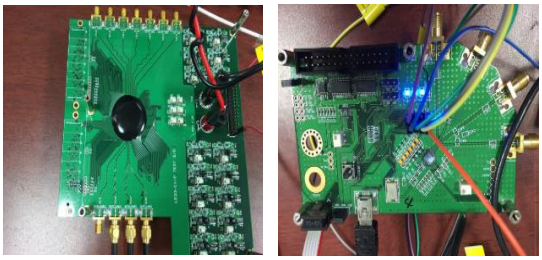

Fig. 19. Test board of the proposed transceiver.

Fig. 19 shows an environment of testing our chip-FPGA connection. We used a SPI protocol for measurement of the chip.

Fig. 20 shows its measured eye diagram at LA output using SPI control. We confirmed that the eye diagram at LA output changes as controlled.

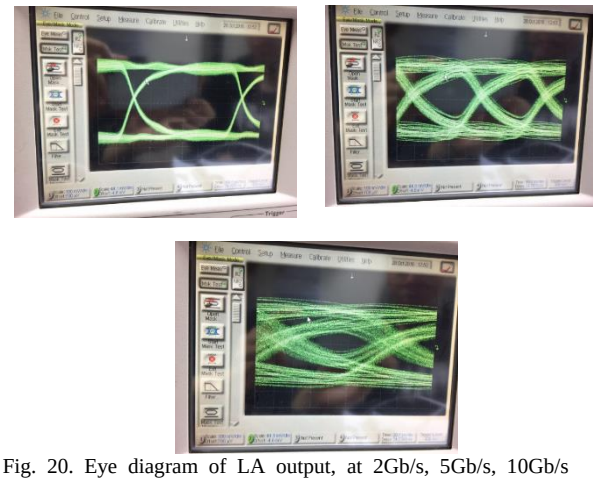

Fig. 20. Eye diagram of LA output, at 2Gb/s, 5Gb/s, 10Gb/s using a SPI

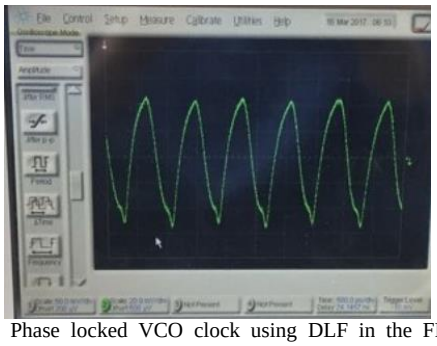

Fig. 21. Phase locked VCO clock using DLF in the FPGA.

Fig. 21 shows phase locked VCO clock using digital loop filter in the FPGA. We confirmed that stable VCO clock is generated through accurate communication between FPGA and chip.

IV. CONCLUSIONS

Using the proposed transceiver, various functions can be implemented by choosing analog blocks in the IC and digital functions in the FPGA and many functions that cannot be verified at the simulation level can be verified in real time, such as Jitter tolerance self-test, Jitter peaking check, Frequency synthesizer, CDR, real-time calibration scheme.

The power consumption of the total chip is 124.35mW at 10Gbps input data and the recovered clock jitter is 2.1ps_{rms} and the total active area is 4mm^2.

ACKNOWLEDGMENT

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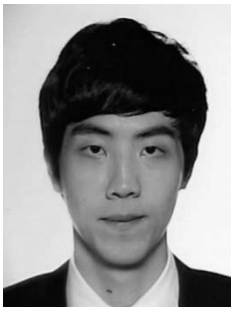

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