Design of FET structure for high frequency in 65nm CMOS process

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Abstract **- New designs of FET are proposed with built-in based and all revised transistor for lower resistance of gate and lower capacitances of C_{gd} to design Millimeter-wave Power Amplifier (PA) for high consistency with simulation. Measured maximum available gain is 9.41dB at 2μm x24 all revised type transistor. The driving voltage of FET is 1.2V and gate voltage is 1V in 65nm normal CMOS process.**

I. INTRODUCTION

The requirements for the applications of the wireless LAN, wireless personal area networks, automotive radar is increasing. Normal CMOS technology is suitable for millimeter wave circuit design due to low prices and high density integration. However, most standard CMOS application is focused at low frequency below than 50GHz. MMICs for high frequency above 50 GHz were presented by SOI CMOS, mHEMT or pHEMT. [1-3] This study has concentrated at low parasitic capacitance and low resistive FET at high frequency above 50GHz and for millimeter-wave in normal CMOS process.

II. DESIGN AND SIMULATION

A. Characteristics of built-in FET by CMOS process

Typical FET manufactured by normal 65nm CMOS process can be used to a long or aspect types in circuit. In this case, an increase in the FET size must inevitably increase the number of finger or increase the finger length. When the length of the finger is increased, the overlap between the source / drain is increased, so that the parasitic capacitance is increased. Conversely, when finger number is increased, the physical path entering each active region from the gate is increased. As a result, it changes the value of the route by R_g. This alters the time to reach the active region, a phase difference occurs. This characteristic is not a problem for low-frequency. However, the difference of driving characteristics generated from the difference of the FET structure will appear larger in the high-frequency.

In addition, increasing the number of via to be connected to the Active region and the source / drain, the size of the area to form one unit channel is increased. And, regardless of the Channel area, the entire area of the FET is increased.

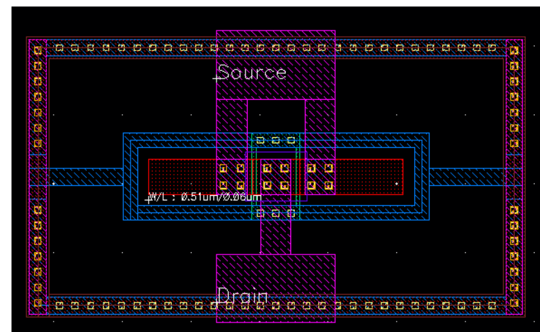

Fig. 1. Built-in FET Type by 65nm CMOS RF process.

Depending on the number of via, the value of the resistance at the electrode of the source / drain is changed in inverse proportion. Therefore, it is not possible to reduce the number of via unconditionally when designing the amplifier. Source resistance and the drain resistance are significantly affect the value of fmax. Especially the source resistance largely exerts an influence on the value of fmax, so it cannot be reduced unconditionally when designing the amplifier.

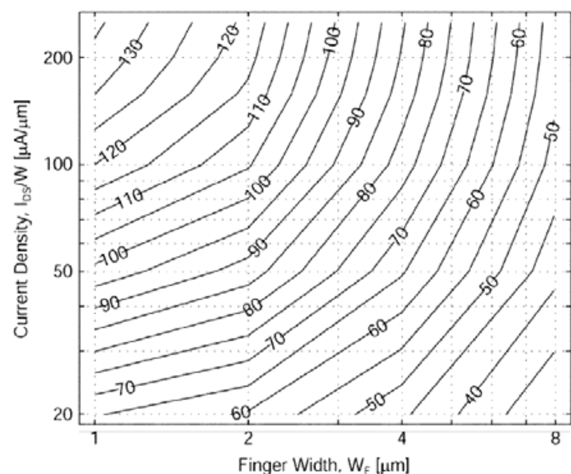

Fig. 2. Measured fmax [GHz] for minimum channel length (L=0.13μm) NMOS transistors. [4]

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Figure 2 shows the fmax distribution of FET different conditions with the same area which was made by 130nm CMOS process. Depending on the number of fingers we can check the fmax vary. [4]

If we want to create a one finger FET in normal 65nm CMOS process, it is not possible to increase the gate finger more than 2um by process limitation. So we have to use multi-finger structure for wide total gate length FET. As we mentioned above, a different phase of the amplification results of each unit channel is increased in accordance with the counts of signal path, gain may be reduced. It is important to select the proper design of the fingers and the outer electrode. RF input signal is connected to the gate electrode for designing a Common Gate amplifier. The design options of gate signal pattern are the one side connection or both sides connection. If the incoming signal is only one side, it is possible to connect the transmission line to the Gate, design is simplified. And the FET itself is aligned in the direction of the signal line.

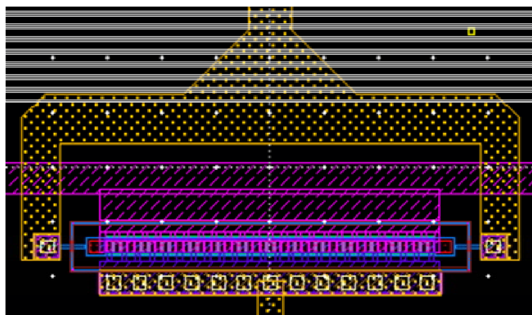

Fig. 3.Vertical connection of multi-finger FET with transmission lines.

Fig. 3 shows both sides connection. When signals are input from both sides, the amplified signal is gathered at the center of the FET. This can be seen as two FETs has half the size of the total gate width. And it is a shape of parallel structure of Gate Resistor, R_g. The physical path from each half active area is shorter than one-side connection, the phase distribution to be reduced. As shown in Fig. 2, the smaller number of finger FET may notice that fmax increases. Both sides gate electrode connecting structure can be a solution by low phase difference. But if total gate width is larger, a path connecting the input signal transmission line with each edge of gate becomes longer. And this makes additional change of the value of LC. The resistance of line can be seen from transmission line varies depending on the LC value. Finally, obtained results of amplifier are different from simulation. On the other hand, we can connect the incoming signal with parallel direction when connecting the input signal. The FET as it has the advantage of changing of the LC is minimized. When using default FET structure provided by the RF CMOS process, there are advantages and disadvantages to each design.

B. Design of FET for high frequency

In this study, we apply the structure dividing of the internal FET with two small FET to solve the issue mentioned in the previous section. First, by default FET structure provided by the RF CMOS process with half of the total desired gate width is designed. The amplified signal comes out from the center.

Since the signal is passed only half of the gate finger, phase change is the half of the conventional structure like horizontally connected FET structure. Further, the parallel structure of the gate electrode can obtain a resistance value ’R_g smaller than conventional. Small resistance value of R_g is better for amplifying by small attenuation before amplifier. Input signal paths are divided by left and right. But if the gate length is not too wider than transmission line width, additional input signal path and its side effects are negligible. If required transistor’s the total gate width is wide enough to use many finger structure, unit gate length can be lengthen to reduce the number of fingers. So in most case, it couldn’t be a problem.

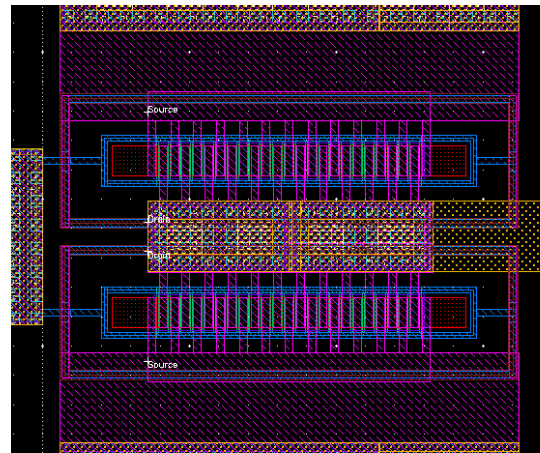

Fig. 4. Dual type FET using built-in FET structure by 65nm CMOS process.

Of course, if the number of fingers to be too large, so a large total width FET is required, modifying wider than the width of the line, but having a less difference than the conventional design. So there is little change in the characteristic of the resistance value caused by difference of LC. Applying the structure that is connected to the left and right source and drain signal was amplified by the designed structure that is output from the center together. Source connecting the left and right outside of the FET, and Drain signal is gathered to come out from the center.

Depending on the built-in FET structure, a gate line structure is utilized only the lowest metal layer of M1. There are the connections surrounding the outskirts of active area and source to form a body by M1, M2. Amplified signal is transferred from the central drain electrode formed by M2 to RF signal metal layer OA.

The source electrode in passing directly below the metal M2 of the drain is connected with the body electrode. This region appears to be an additional value of C_{ds}. It also occurs additionally C_{gs} and C_{gd} by a source and a drain metal electrode directly passing over the gate ring metal M1. This is displayed in proportion to the number of fingers.

In order to operating the FET, Cgs, C_{gd} is required and inevitable. But the basic properties are determined by the intrinsic capacitance value present in the active area. The additional extrinsic capacitances existing outside of active area change in the additional performance. When looking only intrinsic model, in order to operating at high frequency FET transconductance g_m and C_{gs} need to be large. Of

course, if C_{gs} is too large, charging time increases the effect appears that the operating frequency of the FET decreases. But when we consider everything, the ratio of C_{gs} / C_{gd} is important. The higher ratio is needed in the high frequency operation of the FET. That is, it is necessary to design the small value of C_{gd}. This means that the FET will be driven like a linear function that is controlled only by the gate voltage.

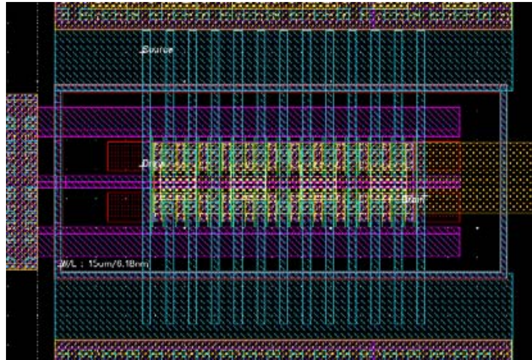

Fig. 5. Dual type FET using different metal layer.

Previously designed FET structure using a default design by CMOS process is a form to improve the properties while maintaining the advantages of the horizontal FET structure in a simple way. However, C_{gd} by the adjacent of the gate and the drain metal is still holding. It is necessary to maximize the distance between the metals in order to decrease C_{gd}. The gate/drain capacitance caused by the drain metal passed over the gate metal ring, so drain electrode in unit FET was formed vertically only above the active area for no overlaps between gate ring and drain electrode. Amplified drain signals from the left and the right half size FET are connected together at M6 metal layer. The increased width of the gate electrode connected to the active region to reduce the R_g that significantly affects the gain of transistor. Width of gate electrode before active area is increased to reduce R_g that significantly affects the gain of transistor, and the number of gate electrode is enlarged from two to three. Center source electrode (ring type) is removed to eliminate central C_{ds}. But each source electrode finger is connected for same voltage level of source. That may increase C_{ds}. Even if the existing feeders in the metal layer M6, connected drain electrode at the center is far from modified source electrode, and extrinsic C_{ds} of this area is smaller. Instead, the two active areas in the p-well are designed closer to each other for same body condition. The outskirt of FET was designed like the ring shape to perform body contact.

III. MEASUREMENTS ENVIRONMENT

The FET and output return loss of the PA with small signal gain achieve through the evaluation S-parameter measurements. The figure below shows the setup for a small signal S-parameter measurement. Vector Network Analyzer up to 70 GHz operating frequency is lower than in Broadband Test Set and because of the additional millimeter-wave Module connection, measuring the frequencies was extended. All the measurements are performed by using the RF probe and the calibration and measurement process.

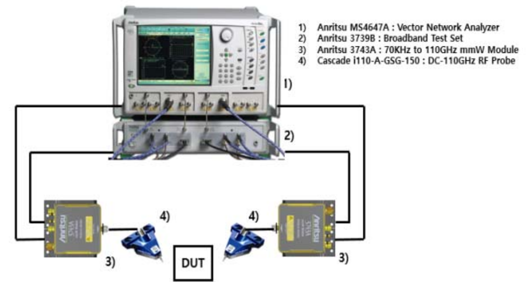

Fig. 6. Environment setup for measuring S-parameter.

Measuring the output frequency and evaluation is possible with the power measurements. First, because the maximum frequency from the PSG Signal Generator cannot output a signal of upper 40 GHz, which can be output high frequency signal with the Source Module is used by the frequency multiplier. Checking the maximum output level of the FET can be performed by the magnitude of the output signal, and also the gain of the circuit can be checked from the difference between the output signal and the input signal.

IV. RESULTS

Measurement was performed at various bias conditions on various transistors. Fig. 7-10 shows S-parameter and MAG data of 2μm x20 dual type transistors at V_{gs} 1V, V_{ds} 1.2V. We can infer R_g and C_{gs} from the S11 graph. If we extend S11 to real Z axis, crossing point is R_g form equivalent circuit. Fig. 7 shows type1 transistor has higher R_g than type 2 transistor. Type 2 transistor has wider electrode and multi metal layer than type 1 transistor, so type 2 transistor has lower R_g than type 1. Also S22 of type 2 transistors shows bigger constant r circle than type 1 transistor. It means higher capacitance value of C_{gs} than type 1. It comes from wide overlap area between wider gate electrode and crossing source electrodes of type 2 transistor.

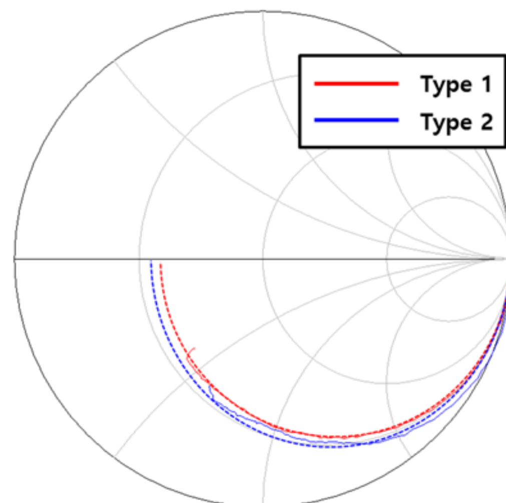

Fig. 7. Measured S-parameter S11 of proposed FETs @ V_{gs} 1V, V_{ds} 1.2V.

Fig. 8 shows measured S22 graph of same bias condition and same transistors with Fig. 7. From S22 characteristic, extended crossing point with real Z axis means R_d. Type 2 transistor has higher R_d value than type 1 transistor. It comes from narrow vertical drain electrodes made by multi metal layer above active area to eliminate overlap electrodes for reducing C_{gd} and C_{ds}. Narrow electrode before wide drain area increases value of R_d. Also type 2 shows low capacitive characteristic. It means lower capacitance value of C_{ds} than type 1 transistor.

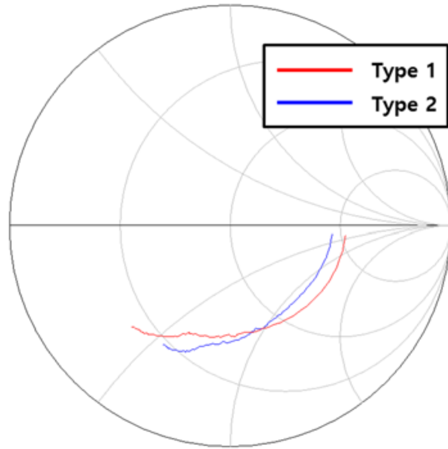

Fig. 8. Measured S-parameter S22 of proposed FETs @ V_{gs} 1V, V_{ds} 1.2V.

Fig. 9 shows measured S21 graph of same bias condition and same transistors with Fig. 7. Low frequency gain of type1 transistor is lower than type 2 transistor. But slope of gain reduction is lower than type 1 transistor. At about 50GHz, S21 values of type 2 is higher than type 1. We can evaluate stability value and maximum available gain of two dual type transistors.

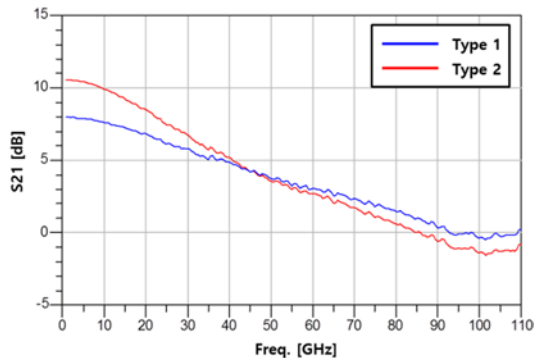

Fig. 9. Measured S-parameter S21 of proposed FETs @ V_{gs} 1V, V_{ds} 1.2V.

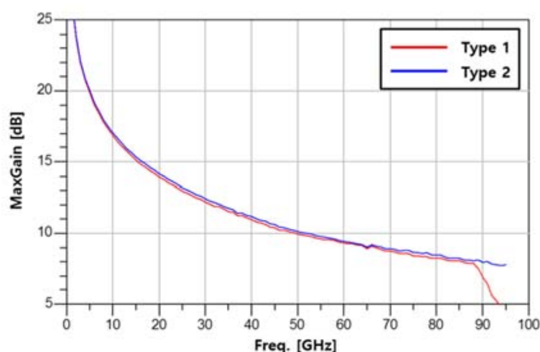

Fig. 10. Measured MAG of proposed FETs @ V_{gs} 1V, V_{ds} 1.2V.

Fig. 10 shows MAG and stability 1 point. Stability 1 point of type 2 is 90GHz, about 10GHz higher than type 1 transistor. If we design power amplifier for 60GHz center frequency, it could operate with ±20GHz bandwidth. So type 2 transistor has enough MAG for high frequency application. Fig. 11 and Fig. 12 show MAG value of various bias conditions with two dual type transistors. Biased conditions are 0.8V/0.8V, 0.8V/1.0V, 1V/1V, 1V/1.2V, 1.2V/1.2V of V_{gs}/V_{ds} at 60GHz in series of graph. Highest gain is obtained at 1V/1.2V condition of 2μm x20 type 2 transistor and gain is 9.16dB. At most bias condition, type 2 transistors show higher maximum available gain. On same bias condition, small finger count of transistor shows higher maximum available gain about 0.12dB at 2μm x24 from the Fig. 11 and Fig. 12.

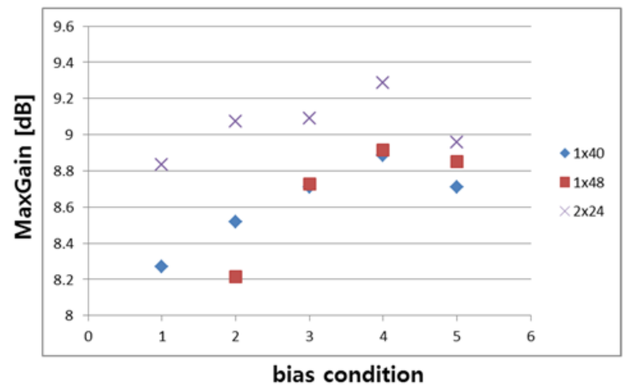

Fig. 11. Measured MAG of proposed type1 FET @ 60GHz, various bias condition.

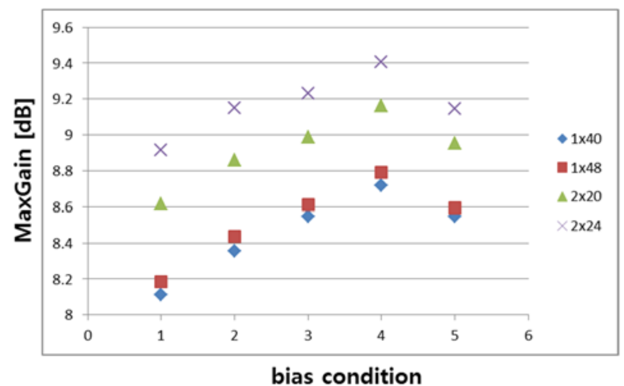

Fig. 12. Measured MAG of proposed type2 FET @ 60GHz, various bias condition.

Fig. 13 and Fig. 14 show fmax frequency at bias condition of 1μm x48 and 2μm x24. Highest maximum available gain (MAG) is 9.41dB at 2μm x24 type 2 transistor and its fmax is also highest about 578GHz (by extrapolation). MAG of 1μm x48 type1 transistor is 8.92dB and fmax is about 475GHz.

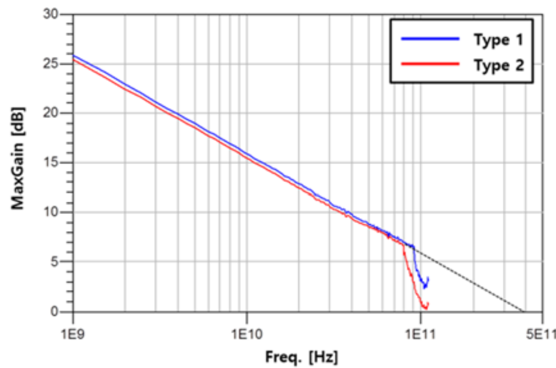

Fig. 13. fmax estimation of 1 m x48 transistors @ V_{gs} 1V, V_{ds} 1.2V.

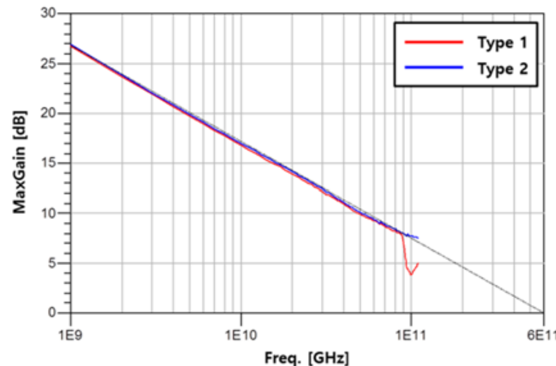

Fig. 14. fmax estimation of 2 m x24 transistors @ V_{gs} 1V, V_{ds} 1.2V.

Table I. shows extracted extrinsic parameter of two types of 2μm x24 FETs after de-embedding method [5-6]. Dual active area type 2 FET shows smaller R_g, C_{gs} and C_{gd} than type 1 FET. These parameters are agreed with design consideration.

TABLE I.
Parameters of 2μm x24 FET

Design Type	Type 1	Type 2
Rg [Ω]	19.64	11.76
Rs [Ω]	5.23	5.98
Cgs [fF]	29.84	21.44
Cgd [fF]	16.06	13.79
Ratio of Cgs/Cds	0.51	0.64
MAG @60GHz	9.29	9.41

V. CONCLUSION

Newly designed transistors are fabricated at normal 65nm CMOS process. Built-in based transistor and all revised transistor are proposed and measured. All revised transistor shows higher gain performance than built-in based transistor. These transistors will be used for designing high frequency power amplifiers.

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REFERENCES

[1] H. Dabag; B. Hanafi; F. Golcuk; A. Agah; J. F. Buckwalter; P. M. Asbeck, “Analysis and design of stacked-FET millimeter-wave power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1543–1556, Apr. 2013

[2] C. Lee; Y. Kim; K. Seo; J. Jeong; Y. Kwon, “A 18GHz broadband stacked FET power amplifier using 130 nm metamorphic HEMTs,” *IEEE Microw. Wireless Compon. Lett.*, vol. 19, no. 12, pp. 828–830, Dec. 2009.

[3] M. Fathi; D. K. Su; B. A. Wooley, “A stacked 6.5-GHz 29.6-dBm power amplifier in standard 65-nm CMOS,” in Proc. *IEEE Custom Integr. Circuits Conf.*, 2010, pp. 1–4.

[4] C. H. Doan; A. M. Niknejad; R. W. Brodersen; “Millimeter-Wave CMOS Design” *IEEE Jour. Solid State Circuits*. Vol. 40, no. 1, pp. 144-155, Jan. 2005.

[5] G. Dambrine *et al*, “A new method for determining the FET small signal equivalent circuit,” *IEEE Trans. Microw. Theory Tech.*, vol. 36, no. 7, pp. 1151–1159, Jul. 1988.

[6] I. Kwon et al., “A simple and analytical parameter-extraction method of a microwave MOSFET,” *IEEE Trans. Microw. Theory Tech.*, vol. 50, no. 6, pp. 1503–1509, Jun. 2002.

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