A Patch-Clamp for detecting the DNA passage

Young Sun Moon[1] and Gyu-Tae Kim[2a]
Department of Micro/Nano System, Korea University[1]
Department of Electrical Engineering, Korea University[2]
E-mail : sjoyfuls@ korea.ac.kr, gtkim@korea.ac.kr

***Abstract* - A patch-clamp circuit of removing the offset with reduced noise was designed and checked in the condition of measuring the ionic current for detecting the passage of DNAs through nano-hole. The significant reduction of noise according to the measurement condition was observed whether the shielding cage surrounds or not, reminding the importance of the extra care for checking the level of the noise. The separation of the command voltage with high input impedance enables the maintenance of the same potential across the counter electrode and the working electrode. The noise level was measured to be around ~ nA, rather higher than the level of the measurement of the DNA passages. The tuning of the offset voltages is needed depending on the electrolyte condition, too.**

I. INTRODUCTION

The identification of the sequence of DNAs becomes more demanding in many fields of the biological application. Even though the time for the DNA sequencing gets shorter, the faster identification is still more desirable. The biological comparison of each acid base in DNAs is based on the comparison with the reference peaks of DNAs. Recently the possibility of the electrical characterization of the DNA bases has been suggested by checking the current of the DNA passage through the nano-hole. With the integrated chip with nano-holes in the solution containing the amplified DNAs, the events of the passage of DNAs through the holes result in the current pulse with the typical heights and widths depending on the driving force in the solution. The low level of the current around ~100pA with 100us of the pulse width requires less noise for reliable determinations. In addition, the offset voltage in the electrolyte solution demands the offset canceling for the better resolution in the measurement setup. Because the voltage can change with the formation of the double layers between the electrodes in the electrolyte, the active clamping of the voltage is crucial to identify the ionic current, requiring a patch-clamp amplifier. In case of patch-clamp, voltage or current are targets of clamp for controlling. The integration of patch-clamp circuits with the offset canceling and reduced noise will enable the fast identification of DNA sequencing by optimizing the measurement signals.

a. Corresponding author; gtkim@korea.ac.kr

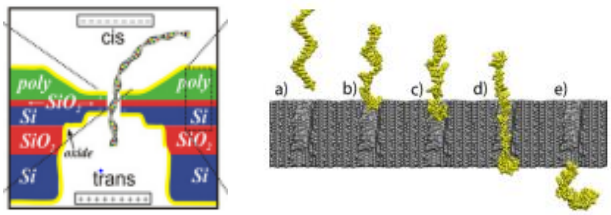


Fig. 1. Schematic diagram of a biosensor consisting of a nanopore in a capacitor membrane, and molecular dynamics of DNA translocation through the pore.[2]

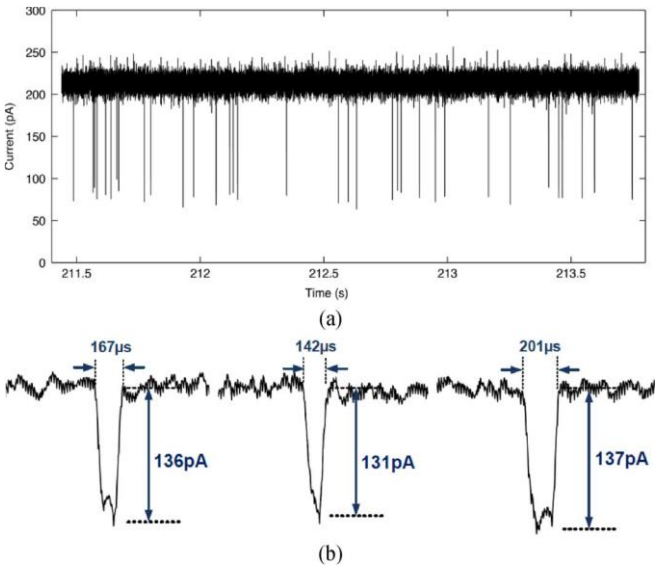
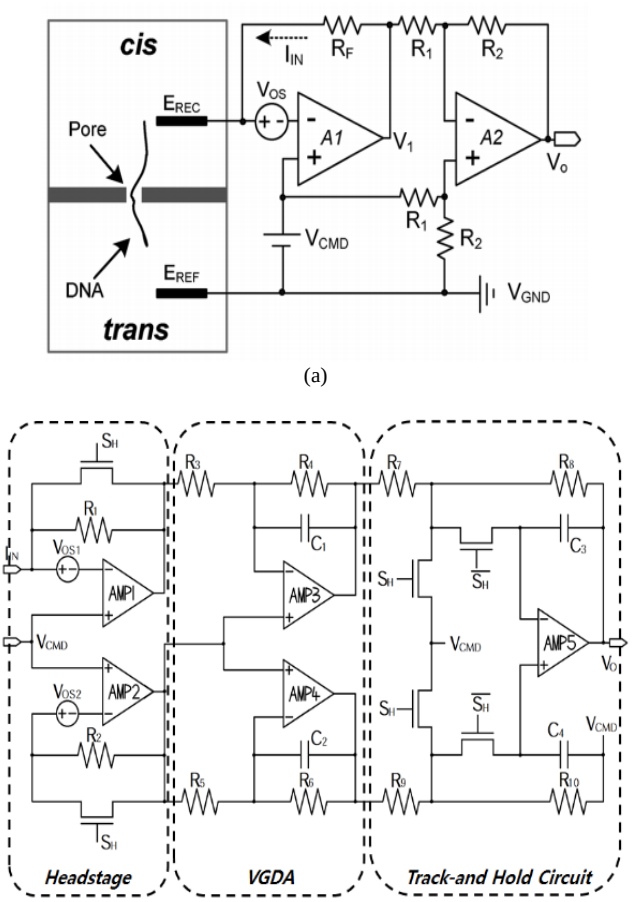


Fig. 2. Examples for identifying DNAs through nano-pore by current measurement.[1]

The wider bandwidth with less noise needs a compromise between the speed and the resolution. The left figure of Fig. 1 denotes the measurement scheme of the ionic current by DNA passages through the nano-holes. Depending on the cis or trans configuration of DNAs, series of the current pulse can be varied owing to the alteration of DNA bases in DNAs.

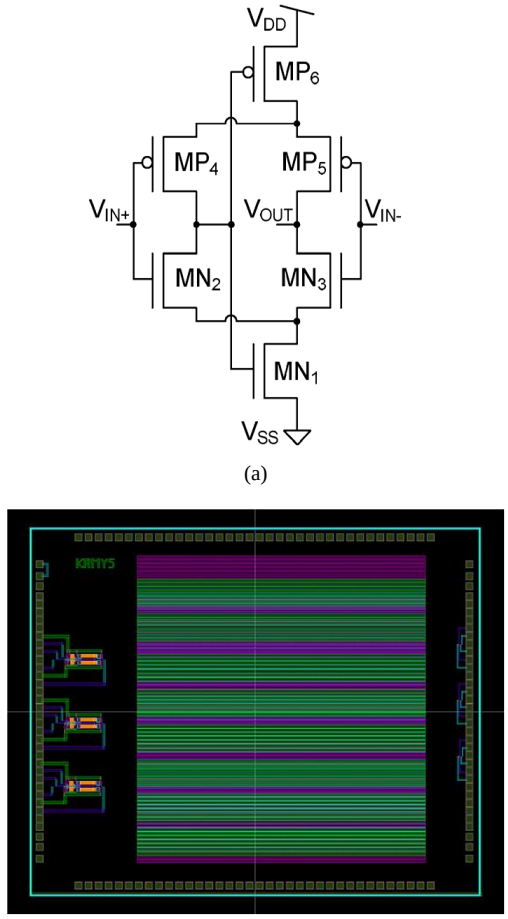
For avoiding the unexpected built-in potential or the spurious current around the conducting substrate, the surface of the chips should be passivated by insulating layers as depicted as yellow lines. The right figure illustrates the step of the DNA passages through nano-hole. For the higher resolution of the signal, the speed of the passage through the hole should be controlled or monitored with better SNR. The



(a)

(b)

Fig. 3. (a) Conventional patch-clamp amplifier setup for detecting DNA passage through the nanopore. (b) Schematics of the patch-clamp designed for Integrated Circuits: headstage, voltage-gain difference amplifier, and track-and-hold circuit.



(a)

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Fig. 4. (a) Circuit of differential amplifier adopted in our circuit design. (b) Layout of the Patch clamp circuit in the Virtuous.

slower speed of the passage makes it easy for identifying the acid base from the electrical signal.

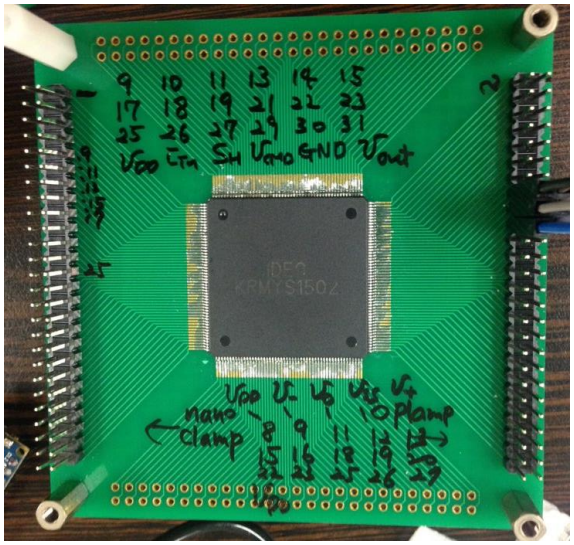
In Fig. 2, Dunbar group et al reported the current pulses with the level of the current pulse about ~125pA and the duration about 200us. Because the DNAs are composed of two helical chains, it should be stripped into single chains with a radius of 1.0nm to enable the passage through nano-holes. One nucleotide unit was measured to be 0.33nm, and comprises the DNAs with millions of nucleotides. Assuming one million number of bases along a DNA chain, the 200us of the current pulse should be distinguished in the interval of 0.2ns, which is not so easy for clearly identifying each base pair owing to the finite bandwidth of the amplifier. So the slowing down of the passage speed of DNA chains through nano-hole are desirable for the better identification. Because the electric field is the main driving force, the alteration of the distribution of the electric field with time can be a good strategy for controlling the speed. The slowdown of DNA passages with wider bandwidth but less noise level is still challenging as an electrical identification tool of DNA sequence. In this report, we reproduced the patch-clamp circuit with less noise and offset canceling following Kim et al[1]. The common mode noise can be rejected by adopting the differential scheme of the input amplifiers. By proper choice of the amplification factor, the compromise between the speed and the better resolution can be optimized.

II. EXPERIMENTS

In our studies, we followed the scheme of Kim et al by the MPW MS350-1502 of IDEC. The function of the patch-clamp amplifier was checked by using the Arduino Pro Mini for generating the pulses of the stimulus signal and NI DAQ as an oscilloscope for monitoring the current level. The spectral response of the amplifier was measured inside or outside of the shielding chamber for comparing with the environmental noise. The signal was compared with the conventional patch-clamp from AXON Instrument.

A. Design of the circuit

Fig. 3 (a) denotes the situation of the DNA passage through nano-hole by the potential of V_{CMD} with the conversion of the current to the voltage followed by the amplification of the voltage signal. Owing to the equipotential feedback between the inverting and the non-inverting terminal of the op amp A1, a driving electric force with the potential of V_{CMD} moves the dipole of the DNAs between E_{REC} and E_{REF}. The output voltage is derived as Eq. (1) with the canceling of the offset voltage and proportional to the input current. By tuning the



(a)

(b)

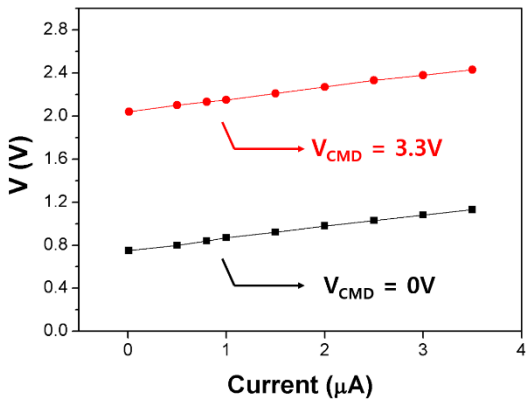
Fig. 5. (a) Test PCB for checking the response of the amplifier. (b) NI DAQ for monitoring the output voltage from the circuits.

ratio of the resistances, the proper amplification factor can be set.

$$V_o = -\frac{R_2}{R_1} R_F I_{IN} \ldots\ldots (1)$$

Fig. 3 (b) is the design we have adopted for the patch-clamp circuit following Kim et al. The patch-clamp circuit is composed of the headstage, the voltage-gain difference amplifier (VGDA), and Track-and Hold circuit. By applying the enabling or disabling signal to the switching transistors of S_H, the circuit switches between the transconductance amplifier and signal capturing circuit. Depending on the threshold voltage of transistors, the proper level of the gate voltages to the transistors should be chosen. In our checks, the function of the transconductance amplifier was good but without the proper function of the signal capturing, which should be improved in the next design.

Fig. 4 depicts the steps which have done by using the Virtuoso Schematic Editor, Spectre, and Calibre. Pre-simulation and post-simulation were done for comparing with the signal from the fabricated chip. For the design of the



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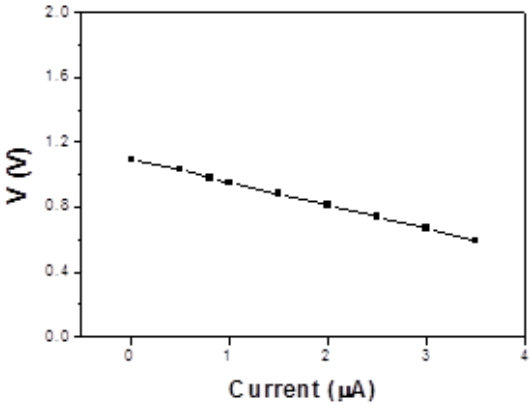

(b)

Fig. 6. (a) Pre-Layout simulation result of the patch-clamp circuit as in Fig. 3. (b) Output voltage vs input current in patch-clamp circuit as in Fig. 3(b).

buffer, the schematic of Fig. 4 (a) was adopted in a differential input with less influence from common-mode noises. Fig. 4 (b) shows the layout of the chips containing three patch-clamp trans-conductance amplifiers and three op-amps. The successful operating part of the circuit was about 1/3, probably damaged during the measurement of the characteristics. In some cases, the failures of the circuit after the measurement were also observed, indicating the susceptible to the electric shock by electrostatic discharges. The protection scheme from the electrostatic shock should be considered in the next design.

The fixed ratio of the resistances should have been designed by some steps for checking the level of the signal.

B. Test condition of the circuit

The chip was packaged in a form of LQFP and mounted as in Fig. 5 (a). The left side of the chip contains three patch-clamp transconductance amplifiers with three op-amps at the right side. The Vcc was applied by the voltage source with the level of 3.3V and the voltage signal was monitored by the NI DAQ with the bandwidth of 10kHz. For simple check of the function, the buffer circuits at the right sides were checked in the measurement of buffering scheme. The overall signal was compared with the pre- or post-simulation results from

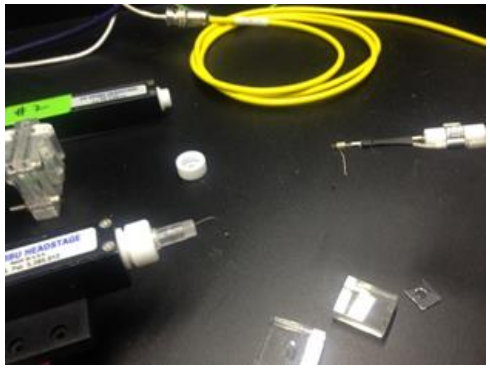

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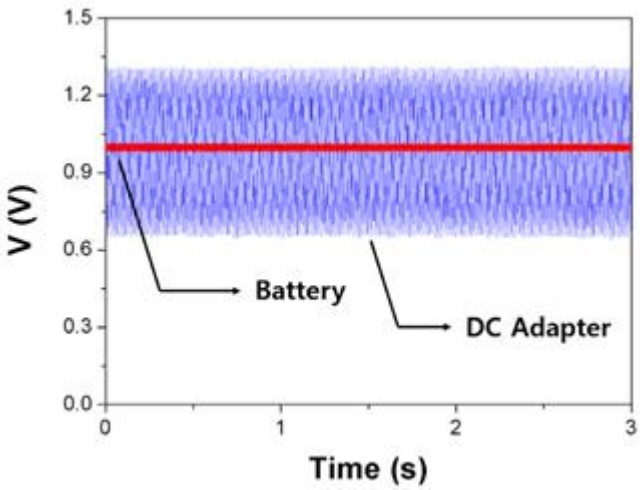
Fig. 7. (a) Cis and trans of patch-clamp system for DNA detection t hrough nanopore by current measurement. (b) Axon DAQ system for current measurement.



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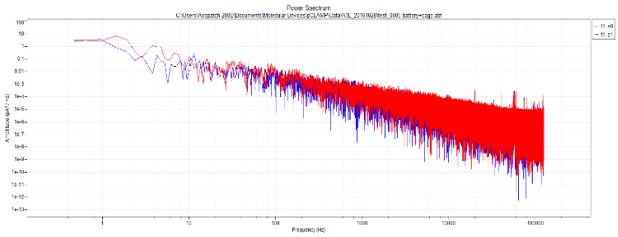

(b)

Fig. 8. (a) Comparison of background voltage signal depending on th e power mode (b) Noise power spectrum of the Patch Clamp Circuit.

the Virtuous. The input current of 1 uA was applied with the voltage source of 1V and the 1MΩ resistor connected to the input port of the patch clamp or the buffer circuit. The driving digital signal fed into S_H was generated by the 3.3V standard Arduino Pro Mini, which can be also possible to operate with 3.0V of mercury battery.

III. RESULTS AND DISCUSSION

A good linear dependency between the input current and the output voltage is desirable for the identification of the current as shown in Fig. 6 (a). In spite of differential input condition in circuit design, the apparent shift of the output voltage in Fig. 6 (a) was expected, which can be understood by the single ended configuration of the measurement. In the experiment, similar shift of the output voltage was also observed. For the better resolution, the check of the differential voltages between the output voltage and V_{CMD} should be done.

Fig. 6 (b) shows the output voltage from the patch-clamp circuit, nicely fitting to the pre-layout simulation in Fig. 6 (a). The negative slope of the output voltage just comes from the opposite definition of the current direction for the measurement. In real situation with DNA passages through nano-holes, the direction of the current flow should be defined by the case of Fig. 3 (a).

To check the noise level of the system, we checked the signal level in the setup of the nanopore measurement as shown in Fig. 7. Fig. 7 (a) shows the probes for the detection of the ionic current resulting from the passage of DNAs and Fig. 7 (b) the measurement setup with Axon DAQs and patch-clamps. The headstage was positioned inside the metal shield cages for reducing the environmental noises, which was confirmed to be very effective for removing the power-noises. The low-pass filter with a corner frequency of 10kHz was also efficient to remove the high frequency noises.

Proper choices of the filter were also important to achieve higher S/N ratio. Because low corner frequency of the low-pass filter can cut the signal pulse or deform the shape of the signal, signal analysis with the filter setting seems to be required.

Fig. 8 (a) shows the significant reduction of the background noise whether the DC adapter or the battery powered. In case of DC adapter, 30times bigger noise level with 60Hz frequency component was observed. With the use of the metal-shield case and the battery power, much reduced noise level was achieved as shown in Fig. 8 (b).

In Table 1, we can clearly see a big advantage of noise reduction by smaller standard deviation of the output signals. So proper shielding with metal-cages and proper grounding will be very helpful for assessing the low level measurements.

But, the noise power spectrum shows much higher levels $\left(S_I = 2.24 \times 10^{-9}\, A/\sqrt{Hz}\ \ at\ \ 10kHz\right)$ than the best target value of $10^{-14}\, A/\sqrt{Hz}\ \ at\ \ 10kHz$[1], which should be improved for ultra-low sensitive measurements.

TABLE I
Statistics on the background voltages from the Patch Clamp Circuit depending on the power mode

Power Mode	Average Voltage (V)	Standard Deviation (V)
DC Adapter	0.9824	0.19717
Battery	0.99798	0.00679

IV. CONCLUSIONS

By IDEC processes, we fabricated the patch-clamp transconductance circuit suggested by Kim et al. A good linear dependence of the input current with the output voltage was confirmed with reduced noise level in the battery-powered and metal-shielded condition, still requiring the improvement of the noise level. Owing to the difference of the design rule such as threshold voltages, the voltage tuning for on/off of the switching transistors was rather difficult, which should be considered for the complete operation of the circuit.

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Gyu-Tae Kim received B.S, M.S and PhD degree in Physics from Seoul National University in 1992, 1996 and 2000. During 2000-2002, he worked as a Humboldt Fellow at the Max-Planck Institute for Solid State Physics in Stuttgart. In 2002, he joined the faculty of Electrical Engineering, Korea University. His research interests include emerging electronic devices such as low-dimensional nanoscale electronic devices, and organic electronic devices.

Young-Sun Moon received B.S degree in electrical engineering from Korea University, Seoul, Korea, in 2013, where she is currently working toward the Ph.D. degree in micro/nano systems. Her research interests include 2-dimensional field effect transistors, and tunneling effect.