Continuous-time delta-sigma modulator using asynchronous SAR quantizer and digital ΔΣ Truncator

Jong Yoon Shin[1] and Sang Gyu Park[a]
Department of Electronic Engineering, Hanyang University
E-mail : [1]sin-0727@hanmail.net

***Abstract* – As the demand for IoT related devices has increased recently, the demand for voice sensors used in these devices is increasing. Low power is a key factor because these devices have to run on batteries for long periods of time. A delta-sigma modulator is best suited for analog-to-digital converters used in the voice signal band because resolution is more important than speed. This delta sigma modulator requires a high SQNR in order to obtain high resolution, indicating that a high bit number quantizer is required. However, a high bit number quantizer requires a large number of comparators and DACs, which increases power consumption and takes up a large area. In this paper, to achieve low noise and low power dissipation, 3rd order continuous time delta-sigma (DS) ADC with a 6-bit asynchronous successive approximation register (ASAR) quantizer and a digital delta-sigma truncator which reduce a number of DACs is presented. The designed ADC front-end has been implemented through a 180 nm CMOS process and achieved 86 dB SNR and 76 dB SNDR over a 20 kHz signal band. The total chip dissipates a power of 170μW from a 1.5 V supply.**

***Keywords*—ASAR quantizer, Audio sensor, Delta-sigma ADC, Truncator**

I. INTRODUCTION

High-resolution delta-sigma modulators have been widely applied to various sensors such as medical instruments, voice sensors, and digital audio. These sensors are applied to a variety of portable devices, which is increasing the need for low power.

The delta-sigma modulator is a type of oversampling A / D converter, which refers to a transducer that samples at a much faster rate than the bandwidth of the signal.

Fig. 1 shows the basic structure of a delta-sigma modulator. The delta-sigma modulator further enhances the signal-to-noise ratio (SNR) by pushing the quantization noise from the signal band to the high frequency band due to the noise shaping characteristic. Since generally the delta-sigma modulators' signal processing is performed in the digital domain, the CMOS process becomes finer and the power consumption is reduced as the driving voltage is lowered. Therefore, a delta-sigma modulator is adopted as a structure of an A/D converter for a voice sensor requiring a relatively small signal bandwidth and a high resolution.

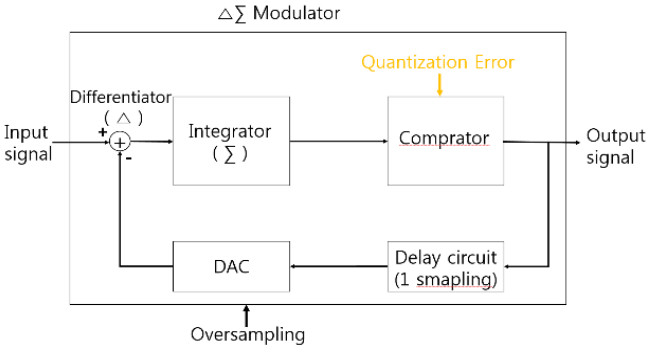

Fig. 1. Structure of oversampling delta-sigma modulator.

The circuit fabricated through this MPW is a low power, high resolution delta-sigma modulator with a signal band of 20 kHz operating on a 1.5V supply. The overall system output has a 16-bit resolution. Table I shows the specifications of this modulator.

TABLE I.
Modulator specification

Parameter	Value
Signal bandwidth	20 kHz
Sampling frequency	1.6 MHz
Resolution	16 bit
Power supply voltage	1.5 V
Power consumption	< 200 μW

The modulator implements a continuous-time delta-sigma modulator to reduce power consumption. The structure of the modulator is a multi-bit third order CIFF (Cascade of Integrators Feed Forward) structure. The oversampling ratio (OSR) was set at 40, which leads to a sampling frequency of 1.6 MHz. The higher the order of the modulator, the easier it

a. Corresponding author; sanggyu@hanyang.ac.kr

Manuscript Received May. 18, 2018, Revised June. 22, 2018, Accepted June. 23, 2018

is to obtain high resolution, but a disadvantage is that it becomes difficult to ensure the stability of the system. Using a multi-bit quantizer, the modulator can be operated at a lower OSR compared to those using a single bit quantizer, and the quantization error is reduced to improve the signal to quantization noise ratio (SQNR).

In the CIFF architecture, the output swing range of the integrator is reduced. This has the advantage that the design conditions of the op-amp in the integrator are relaxed [1].

Fig. 2 shows the block diagram of the continuous-time delta-sigma modulator used in this design. Table II shows the parameters used in this work. The modulator's coefficients were determined after extensive MATLAB behavioral simulations to achieve a SQNR greater than 115 dB, which is 20 dB larger than the target SNR. In a delta-sigma modulator, the input-referred noise of the first integrator is added directly to the input signal and is not reduced by the noise shaping of the modulator. Therefore, the flicker noise was suppressed by increasing the size of the transistors in the OP-amp for the first integrator. We also applied the data weighted averaging (DWA) technique to reduce the nonlinear distortion of the output of the 9-level DAC caused by the mismatch between the eight DAC units.

When using a continuous-time delta-sigma modulator, there is a problem that excessive loop delay (ELD) changes the transfer function of the modulator [2]. The ELD is caused by the delay between the sampling instants and the time where DAC output is available. To prevent this modification of the transfer function by ELD, an additional DAC is implemented in the input path of the ASAR quantizer. This second DAC cancels the effect of ELD so that the desired transfer function is maintained.

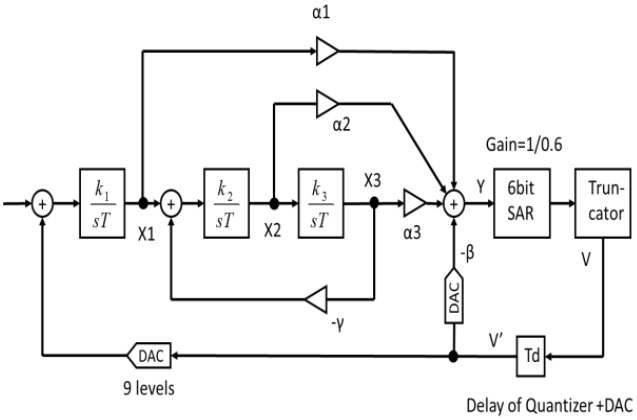

Fig. 2. Structural diagram of the 3rd order CIFF delta-sigma modulator.

TABLE II.
Delta-Sigma Modulator Parameters

a1	15.805	k1	1
a2	37.748	k2	0.25
a3	54.758	k3	0.0625
γ	0.2368		

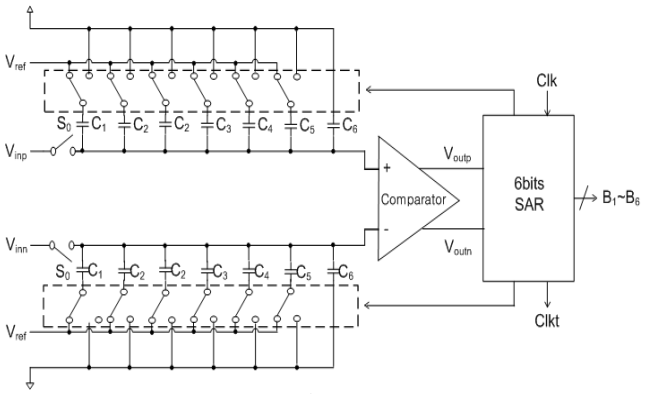

Fig. 3. Schematic of 6-bit ASAR quantizer.

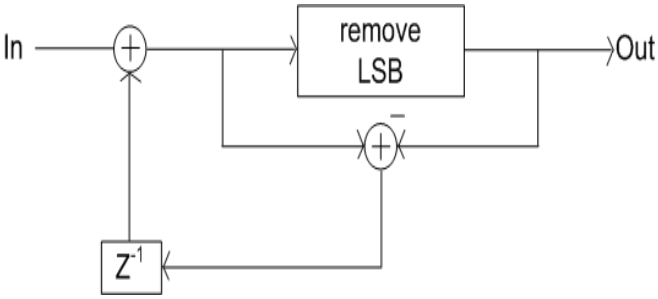

Fig. 4. Block diagram of digital delta-sigma truncator.

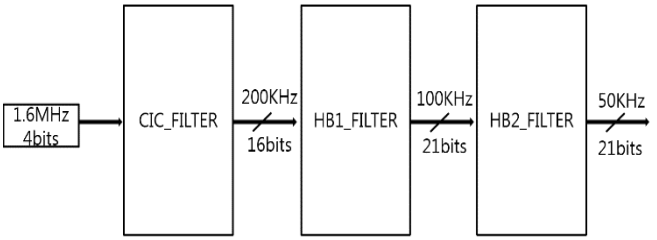

Fig. 5. Block diagram of decimator.

To achieve a high SQNR, a 6-bit quantizer is used. If the 6-bit quantizer is implemented as a flash ADC, 63 comparators are required. This occupies a considerable area, and the power consumption resulting therefrom is also significant. Also, there is a problem that distortion occurs due to mismatch between 63 comparator units. Therefore, this design employed a 6-bit asynchronous SAR quantizer [3]. Fig. 3 shows a schematic of the quantizer used in this work. The ASAR ADC employed set-and-down monotonic switching scheme proposed in [4].

If the 6-bit output of the quantizer is directly used as the feedback signal, a 6-bit DAC with 63 unit DACs are needed. This leads to problems of a large area and large power dissipation. In this work, we used a digital delta-sigma modulator to truncate the 6-bit quantizer output to a 9-level output. Because of the noise shaping, the in-band truncation error can be minimized. Behavioral simulations show that the SQNR degradation from the truncation is very small. Fig. 4 shows a block diagram of the 9-level digital delta-sigma truncator in the modulator [5].

The performance of the op-amps used in the integrators was determined considering the OSR, sampling frequency and power consumption, and is specified to have a gain of more than 40 dB, a trans-conductance of more than 1mA/V, and a power consumption of less than 40 μW. The op-amp used a general 2-stage structure and reduces the transistor size of the remaining op-amps except for the first op-amp to reduce power consumption.

In this work, we implemented a decimation filter which convert the 9-level, 1.6MHz output from the truncator to a 16-bit, 50 kHz signal. When the decimation filter reduces the sampling speed of the signal, it also low-pass filter the signal so that the quantization noise in the high frequency region is removed. Fig. 5 shows a block diagram of the decimator used in the modulator. It consists of one cascaded integrator-comb (CIC) filter and two finite impulse response (fir) filters used as half band filters. The CIC filter reduces the sampling rate to 200 kHz and the two half band filters lowers the rate to 100 kHz and 50 kHz, respectively.

II. EXPERIMENTS

A. Specification

After setting the target specification, the design determines the parameters to achieve this through extensive behavioral simulations using MATLAB. We started simulations with ideal integrators, ideal quantizer and ideal DAC. Fig. 6 shows the results obtained from a MATLAB behavioral simulation of the delta-sigma modulator. It can be observed that the power is concentrated at the input signal of 4 kHz and the noise in the vicinity is shaped. With a signal band of 20kHz and an operating frequency of 1.6MHz, the SQNR was measured to be about 117 dB which is 27dB higher than the target SNR of 90dB.

Then we proceeded to include the effects from various non-idealities such as finite op-amp gain, finite op-amp bandwidth and mismatches.

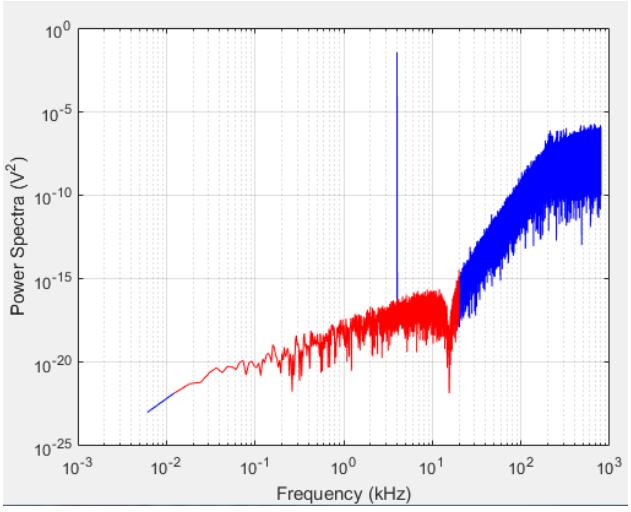

Fig. 6. Power spectra of delta-sigma modulator from a MATLAB simulation. Input : f_{sig}=4kHz, 900mV(-4.4dBFS)

B. Simulation

The proposed delta-sigma ADC was implemented through a 180 nm 1P6M CMOS process from MagnaChips. The CAD tools used in above process are shown in Fig. 7. Based on the parameters determined at the Specification stage, the sub-blocks constituting the delta-sigma modulator was implemented. For the design of analog parts including integrators, a comparator, and a DAC, Specter from Cadence was used. For the design of the digital part, VCS from Synopsys was used, which produces Verilog code for the digital part.

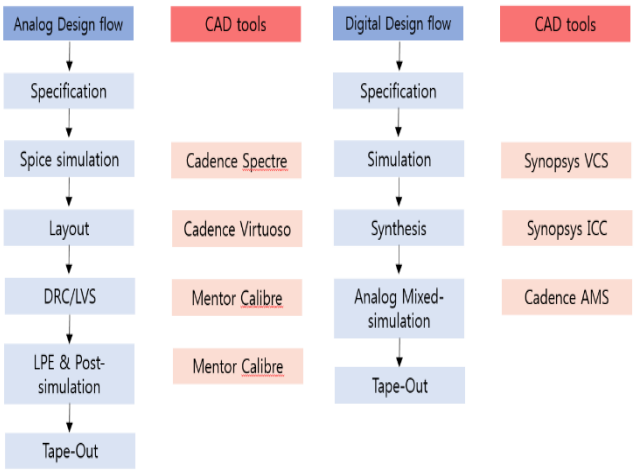

Fig. 7. Design flow and CAD tools

C. Layout/Synthesis

After obtaining the desired specification of an analog schematic and digital Verilog code through spice simulation and VCS, the layout was arranged. The layout of the analog part was done using Cadence's Virtuoso and the layout of the digital part was done using digital synthesis tool IC Compiler from Synopsys. In order to mitigate the mismatch caused by the wafer's gradient and other effects, we paid special attention. For op-amp input pairs, DAC units and, comparator input pair, we employed common-centroid layout, and we used dummy components where the matching is important.

Fig. 8 shows the layout of the capacitor array in the ASAR 6-bit quantizer. It has 64 capacitors, of which 32 were used and the rest were dummies. The colored rectangles represent capacitors of 16C, 8C, 4C, 2C, C and C, which is placed by common centroid.

Fig. 9 shows the layout of the ADC core. The size of the layout is 0.8mm x 0.8mm. Fig. 10 shows the layout of the decimator. The size of this layout is 0.86mm x 0.86mm. Note that the layout of the decimator was done using IC Compiler from Synopsys.

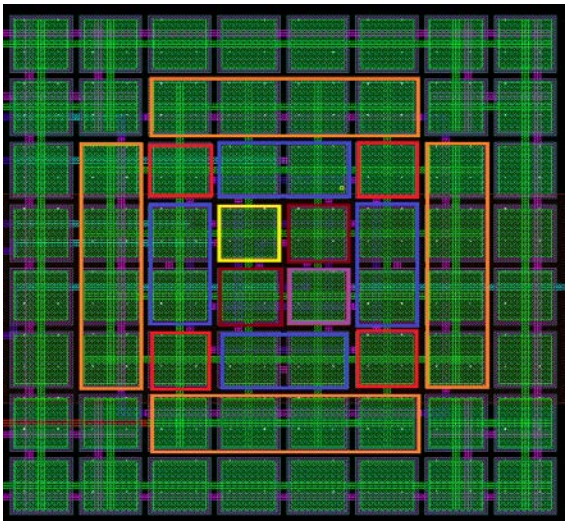

Fig.8. Layout of the capacitor array used in the ASAR quantizer placed by common centroid method.
(Orange: 16C, Blue: 8C, red: 4C, Purple: 2C, Yellow and Pink: C)

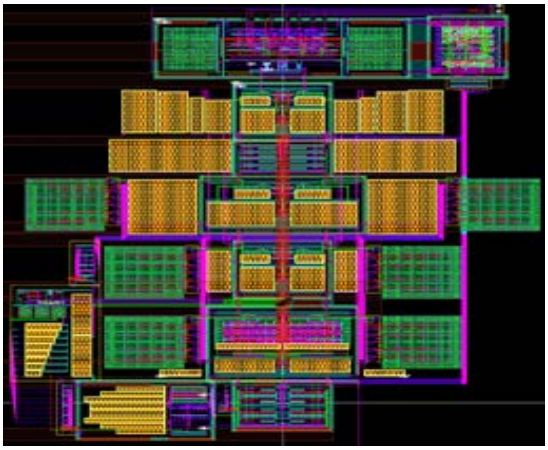

Fig. 9. ADC core layout

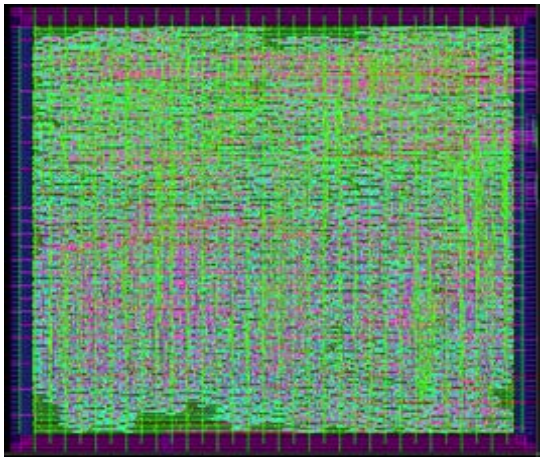

Fig. 10. Decimator layout

In this work, we included test patterns to test each sub-block of the modulator independently, and confirms how each sub-block affected the overall performance after chip design.

D. DRC/LVS

Mentor's Caliber DRC confirms violation of the design rule, and Caliber LVS verified whether it was consistent between schematic and layout.

E. LPE & Post-layout simulation

After verification with DRC and LVS, Mentor's Caliber extracted parasitic R and C values caused by layout and performed post-layout simulation on the netlist including them.

F. Analog Mixed-simulation

Through the synthesis process, the IC Compiler optimized the synthesis of the digital part. After that, it was important to verify that the digital part functions with the analog part correctly. Especially, to take into the delays of the digital part was important. To verify that, we performed analog mixed simulations using AMS from Cadence.

G. Measurements

The measurement setup is shown in Fig. 11. A fabricated chip was mounted on a PCB with chip-on-board (COB) technique. A supply voltage of 1.5V was applied using a N6781 power supply. The ADC input signal and the clock was generated by AP-2700 audio analyzer from Audio Precision. The single-ended input signal from the AP-2700 was converted to a differential signal via a transformer and input to the test board. The digital output of the delta sigma ADC was acquired by 16801A logic analyzer. The collected data was analyzed using MATLAB.

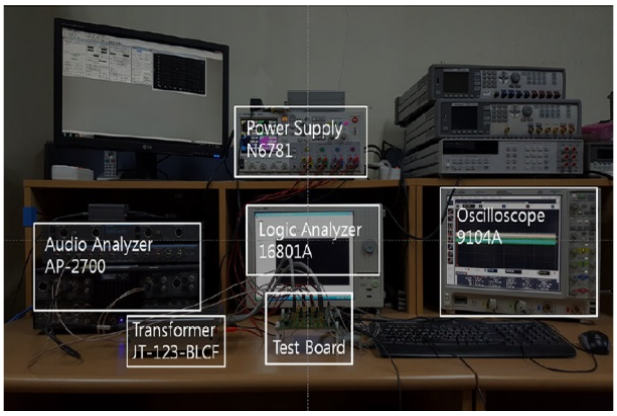

Fig. 11. Measurement environment.

III. RESULTS AND DISCUSSION

Fig. 12 shows the SNR as a function of the input amplitude. The input frequency was 1 kHz. We can observe a peak SNR of 86.4 dB at -1dBFS. Fig. 13 shows the SNDR vs input amplitude. We observe a peak SNDR of 75.7dB. The maximum SNDR was more than 10 dB lower than the maximum SNR due to the nonlinearity in the loop. The power consumption of the chip was 170μW from a 1.5V supply.

Table III shows Performacne summary of the ADC.

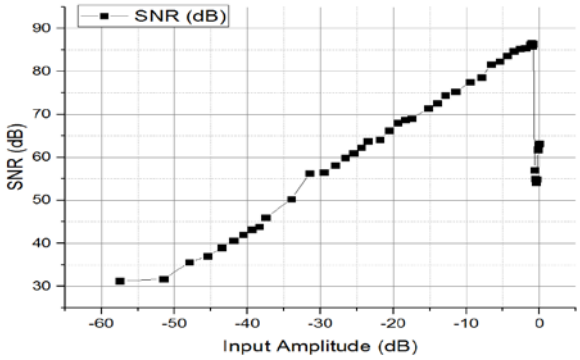

Fig. 12. Input vs SNR

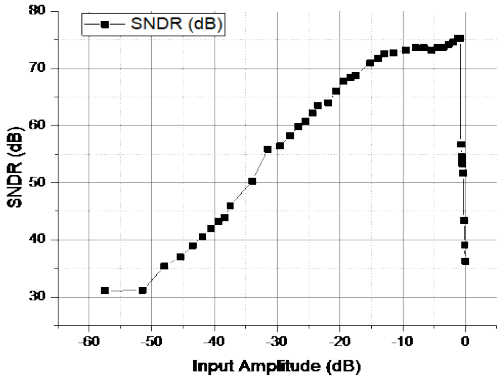

Fig. 13. Input vs SNDR

TABLE III.
Performance Summary

Tech.CMOS	180nm
Fs (MHz)	1.6
BW (KHz)	20
OSR	40
Peak SNR (dB)	86.4
Peak SNDR (dB)	75.7
Area (mm^2)	1.38
POWER (mW)	0.17
V_{DD}	1.5

IV. CONCLUSION

In this work, we developed a 3rd-order CT DS-ADC with a 6-bit ASAR quantizer and a digital delta-sigma truncator. The designed ADC front-end was implemented using a 180 nm 1P6M CMOS Process. It achieved an SNR of 86 dB and an SNDR of 76 dB over a 20 kHz of signal band. The total chip dissipates a power of 170 μW from a 1.5 V supply.

REFERENCES

[1] Schreier, R., & Temes, G. C. (2005). Understanding delta-sigma data converters. Piscataway: IEEE Press.
[2] Ortmanns, M., & Gerfers, F. (2006). Continious-time sigma-delta A/D conversion. Springer.
[3] Yafei Ye, “A 120dB SNDR Audio Sigma-Delta Modulator with an Asynchronous SAR Quantizer”, Circuits and Systems (ISCAS), 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, South Korea.
[4] C-C Liu, S-J Chang, G-Y Huang, Y-Z Lin, “A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure,” IEEE J. Soli-State Circuits, Vol. 45, pp. 731-740, 2010.
[5] Hung-Chieh Tsai, “A 64-fJ/Conv.-Step Continuous-Time ΣΔ Modulator in 40-nm CMOS Using Asynchronous SAR Quantizer and Digital ΔΣ Truncator”, IEEE Journal of Solid-State Circuits, vol. 48, Issue: 11, pp. 2637-2648, Nov. 2013.

Jong Yoon Shin received the B.S. degree in electronic engineering dept. from Hanyang University, Seoul, Korea in 2017 and is currently working toward the M.S. degree in electrical electronic computer engineering dept. from Hanyang University, Seoul, Korea. His main interests are delta-sigma ADC.

Sang Gyu Park received B.S. and M.S. degrees in electronics engineering from Seoul National University, Korea, in 1990 and 1992, respectively, and a Ph.D. degree in electrical and computer engineering from Purdue University, Indiana, U.S., in 1998. From 1998 to 2000, he was with AT&T Laboratories-Research, where he conducted research on high speed optical transmission systems. In 2000, he joined the faculty of the Department of Electrical and Computer Engineering of Hanyang University, Seoul, Korea, where he is now a professor in the department of electronic engineering. His current research interests include mixed-signal CMOS integrated circuits, CMOS sensor circuits, and optical fiber transmission systems.