Two-Stage Distributed Amplifier and Cascaded Single-Stage Distributed Amplifier in 65 nm CMOS Process

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Abstract **– This work presents a 2-stage distributed amplifier (DA) and a 2-stage cascaded single-stage distributed amplifier (CSSDA) in Samsung 65 nm CMOS technology. They are designed in cascode configuration to obtain broad bandwidth and high gain, and m-derived filter configuration is used for compact layout. The measurement results show a peak gain of 10 dB of 2-stage DA and 13 dB of 2-satge CSSDA with the 3-dB bandwidth from 5 GHz to 20 GHz. S11 and S22 are better than -10 dB over the entire bandwidth. The chip sizes are 720 × 540 μm² and 580 × 450 μm² for the 2-stage DA and the 2-stage CSSDA, respectively.**

I. INTRODUCTION

Recently, as the era of Internet of Things (IoT) comes, the need for high-speed, high-capacity data transmission is increasing. The demand for broadband communication systems will continue to increase. In particular, broadband circuits are a key building block in various fields such as high-speed communication, high-frequency instrumentation devices and high-resolution imaging systems. Broadband amplifiers are an essential circuit block for such high-speed applications [1]-[3].

Distributed amplifiers have been popularly employed for broadband applications for their wideband characteristics. In this paper, distributed amplifiers in two different configurations are designed and fabricated in 65 nm CMOS, with the design emphases on low power and small chip area, for possible application to IoT devices.

In Section II, the overview of conventional distributed amplifier (DA) and cascaded single-stage distributed amplifier (CSSDA) is presented. Section III describes the design of 2-stage DA and 2-stage CSSDA. In Section IV, discussions on the measurement results are presented.

II. BACKGROUND

A. Conventional Distributed Amplifier (DA)

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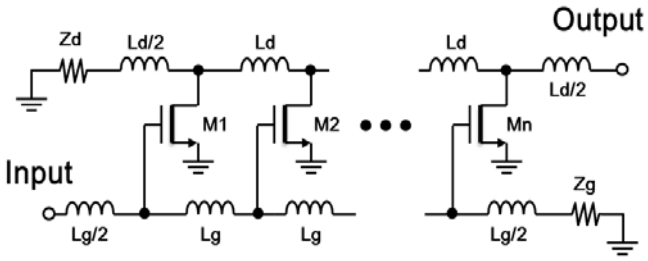


Fig. 1. Schematic of conventional distributed amplifier.

The bandwidth of resistively-loaded amplifiers is typically limited by gate and drain capacitance of transistors. In contrast, conventional DA uses a distributed matching technique where the input and output capacitance of a transistor can be absorbed by series inductors to form input and output artificial transmission lines, thereby providing wideband input and output impedance matching.

Fig. 1 shows the conventional structure of a distributed amplifier in common source configuration. Inductors in the input and output artificial transmission line absorb the gate and drain capacitance of the transistors. In the input transmission line, input voltage wave is travelling and generating drain voltage waves, which are eventually combined in-phase at the amplifier output terminal. The signals reflected in the opposite direction of the input and output lines generate gain ripples and degrade input and output return losses. Therefore, the input and output lines must be terminated by a resistor matched to the characteristic impedance of each line, to absorb incoming waves and thus to eliminate reflection. If the gate and drain capacitance of the transistors are C_g and C_d, respectively, the characteristic impedances of the input and output artificial transmission lines with L_g and L_d can be expressed by Equation (1) and (2) [4].

$$Z_g = \sqrt{\frac{L_g}{C_g}} \tag{1}$$

$$Z_d = \sqrt{\frac{L_d}{C_d}} \tag{2}$$

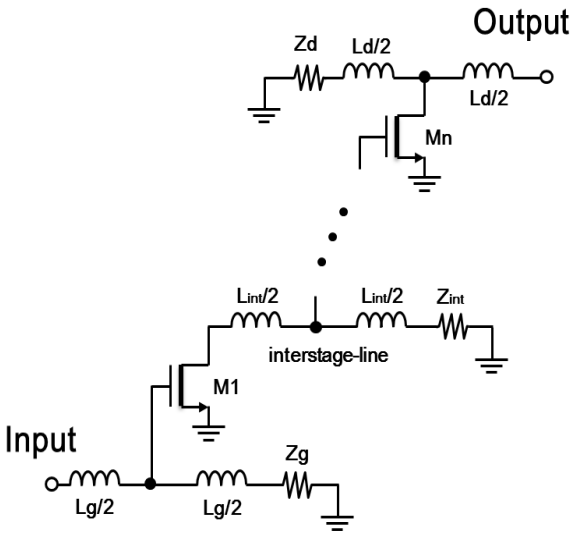


Fig. 2. Schematic of CSSDA.

The maximum gain at low frequencies is given in following Equation (3).

$$A_v = \frac{1}{2}\ n\ g_m\ Z_d, \tag{3}$$

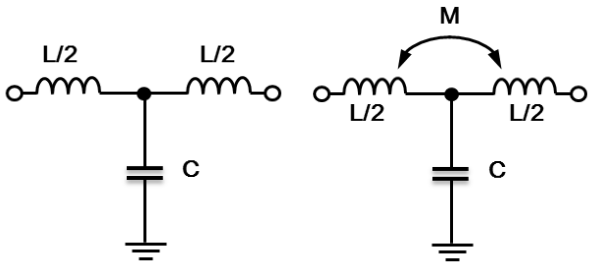
where n is the number of distributed stages and g_m denotes the transconductance of each stage (the source impedance is assumed to be matched to Z_g).

Conventional DA's exhibit wide bandwidth, high reverse isolation, and in general sufficient stability. However, due to the gate resistance of the transistors, the input line may have relatively high attenuation, resulting in amplifier gain reduction, especially at high frequencies [5]. In general, drain capacitance of CMOS transistors are smaller than the gate capacitance. Therefore, in order to make time delay of gate and drain line equal, additional capacitance is necessary at every drain node. Otherwise, the input and output lines may have different time delay per section, and therefore the output signals from each stage may not combine in-phase at the amplifier output, resulting in non-optimal gain.

B. Cascaded Single-Stage Distributed Amplifier (CSSDA)

Fig. 2 is a schematic of a CSSDA [6], which has the potential for higher gain than conventional DA. By cascading multiple DA's, wide bandwidth and high gain characteristics are achieved. The gain of conventional DA is increased in proportion to the number of stages, *n*, as shown in Equation (3), but the gain of CSSDA is increased exponentially with the number of stages, *n*, as shown in Equation (4) [7]. This CSSDA property makes it possible to realize higher gain with lower number of stages compared to a conventional DA, which is especially useful in CMOS processes where transconductance is typically low. The low-frequency gain of a CSSDA is given as follows.

$$A_v = \frac{1}{2}\ g_m^n\ Z_{int}^{n-1}\ Z_d \tag{4}$$



(a) Constant-k filter (b) m-derived filter

Fig. 3. Structure of artificial transmission line.

In Equation (4), Z_{int} is the characteristic impedance of the inter-stage artificial transmission line. Higher values of Z_{int} in general will yield higher low-frequency gain, but at the expense of lower cutoff frequency.

In conventional DA, phase matching is required between the input and output lines as described above, but in CSSDA, there is no need for such phase matching since there is only one signal path from the input to the output.

C. Structure of artificial transmission line

There are two filter structures popularly used in the artificial transmission line: one is a constant-*k* filter, and the other is an *m*-derived filter [8]. The constant-*k* filter consists of series inductance and shunt capacitance as shown in Fig. 3 (a). The cutoff frequency, f_c, of this structure is given by Equation (5).

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{5}$$

An *m*-derived filter is similar to the constant-*k* filter structure, but has mutual inductance between the two inductors, as shown in Fig. 3 (b). The cutoff frequency of this structure is given by

$$f_c = \frac{1}{\pi\sqrt{LC(1+k)}}, \tag{6}$$

where k is coupling coefficient and M is mutual inductance. Since the coupling coefficient k is negative for the series-aiding connection, the cutoff frequency of *m*-derived filter is higher than that of constant-*k* filter for same LC product.

III. DESIGN

A. 2-stage DA

In this paper, we designed a 2-stage conventional DA using the cascode structure in 65 nm CMOS as shown in Fig. 4. Cascode structure is in general suitable for distributed amplifiers due to their relatively high maximum available gain, high reverse isolation, stability and high output resistance. In addition, cascoding also reduces the Miller effect which may otherwise limit the bandwidth [9].

In order to increase the bandwidth and improve the return

loss, an *m*-derived filter was used instead of the constant-*k* filter in the artificial transmission line. The two coupled inductors in the *m*-derived filter can be implemented by a single inductor with a center tap, which reduces the total inductor area by up to 40% compared to a constant-*k* design.

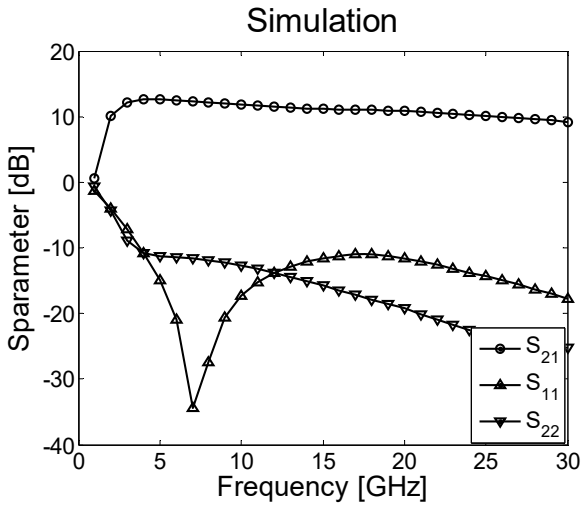


Fig. 4. Simulation results of the designed 2-stage DA.

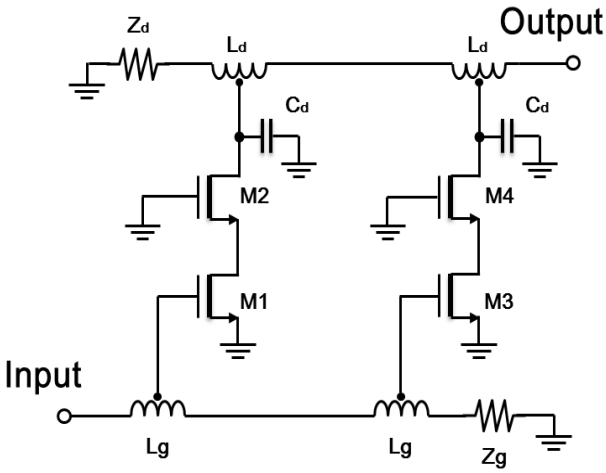


Fig. 5. Schematic of the designed 2-stage DA in 65 nm CMOS process.

Fig. 5 shows simulated performance of the designed 2-stage DA. All layout parasitics are carefully modeled by Advanced Design System (ADS). The 3 dB bandwidth of the 2-stage DA is from 4 GHz to 28 GHz with 12 dB peak gain. The S_{11} and S_{22} are better than -10 dB within the 3dB-bandwidth. The designed amplifier consumes 110 mW of dc power with 46 mA of the total drain current.

B. 2-stage Conventional Cascaded Single-Stage Distributed Amplifier (2-stage CSSDA)

In addition to the 2-stage conventional DA, 2-stage CSSDA is designed in 65 nm CMOS as shown in Fig. 6. The designed CSSDA employs cascode structure for the same number of transistors, and the input and output artificial transmission line uses the *m*-derived filter instead of constant-*k* filter.

The designed 2-stage CSSDA is implemented with stacked inductor shown in Fig. 7, which has a smaller footprint than a non-stacked inductor. Stacked inductor, while providing higher inductance than a non-stacked one for the same area, may have lower quality factor due to relatively high resistive loss [10].

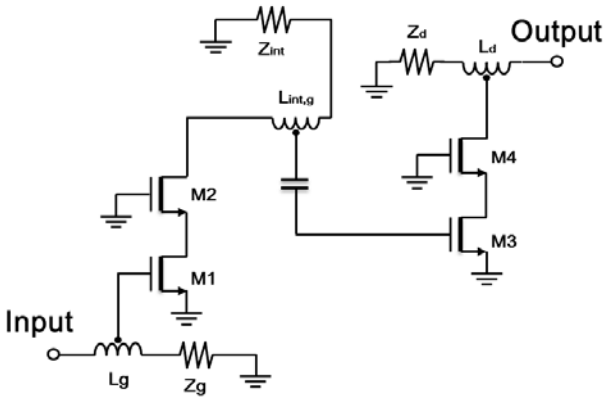


Fig. 6. Schematic of the designed 2-stage CSSDA in 65 nm CMOS process.

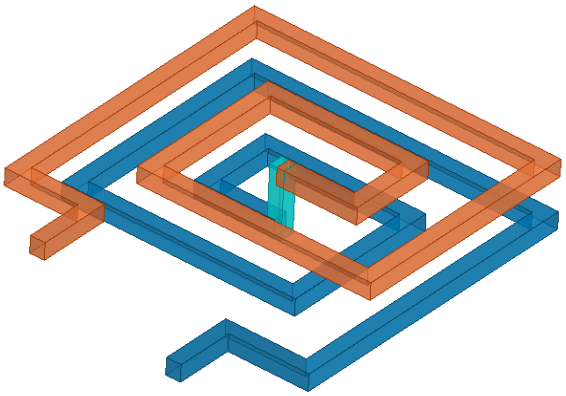


Fig. 7. Layout of stacked inductor.

Simulated performance of the designed 2-stage CSSDA is shown in Fig. 8. The 3 dB bandwidth is from 4 GHz to 26 GHz with peak gain of 15 dB. The S_{11} and S_{22} are better than -10 dB within the 3 dB bandwidth. The total drain current is 45 mA similar to the 2-stage CDA and the dc power consumption is 63 mW.

IV. RESULTS AND DISCUSSION

The designed 2-stage DA and 2-stage CSSDA are fabricated in 65 nm CMOS process. The *S*-parameters of the designed circuits are measured from 1 GHz to 30 GHz using on-wafer testing setup with Anritsu VNA. The measurement results are shown in Fig. 9. The peak gain of the 2-stage DA and the 2-stage CSSDA are measured to be 10 dB and 13 dB gain, respectively, which are lower than the simulation by approximately 3 dB. The 3 dB bandwidth is measured to be from 5 GHz to 20 GHz, which are narrower than the simulation. The discrepancy from the simulation is believed

to be due to random process variation and modeling inaccuracies. Measured S_{11} and S_{22} were below -10 dB from 4 GHz to 22 GHz.

The measured results confirm that the gain of the 2-stage CSSDA is higher than the 2-stage DA by 3 dB, while consuming only 60% of the dc power, as simulation

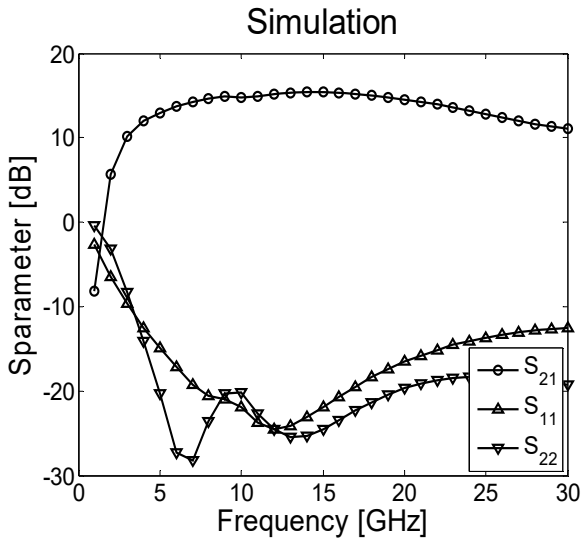


Fig. 8 Simulation results of the designed 2stage-CSSDA.

predicts.

The performance advantage of the CSSDA compared to DA, in terms of high gain and low dc power consumption, will be even greater if more than two stages are cascaded.

Fig. 10 shows chip photographs of the 2-stage DA and 2-stage CSSDA fabricated in this work. The chip sizes are 720 × 540 μm^2 and 580 × 450 μm^2 for the 2-stage DA and the 2-stage CSSDA, respectively. The 2-stage CSSDA occupies only 65% of the chip area of the 2-stage DA since stacked inductors are used and no additional capacitors are necessary on the drain nodes for phase matching.

Comparison with other CSSDA is shown in Table I. The distributed amplifiers in this work have smaller area and lower dc power consumption.

TABLE I.
Performance comparison table.
Chip sizes are measured excluding pads.

	Process	Gain (dB)	BW (GHz)	PDC (mW)	Chip Area (mm^2)
[11]	0.18μm CMOS	25	1.5-35.5	176	0.86
[12]	0.18μm CMOS	20.5	35	250	0.78
This Work DA	65nm CMOS	10	5-20	110	0.39
This Work CSSDA	65nm CMOS	13	5-20	63	0.26

V. CONCLUSIONS

In this paper, 2-stage distributed amplifier and 2-stage cascaded single stage distributed amplifier are designed in 65 nm CMOS process, and measured by on-wafer testing

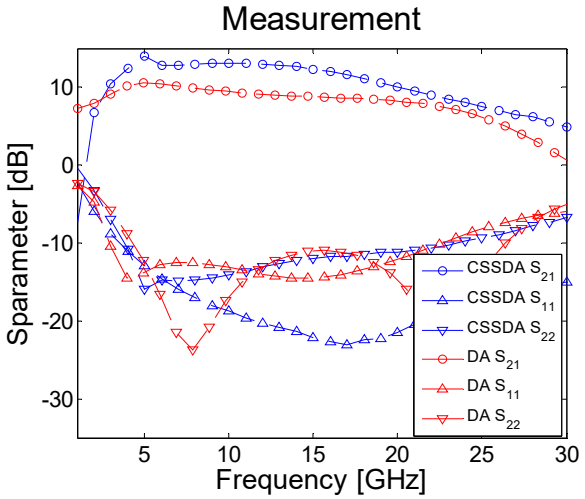
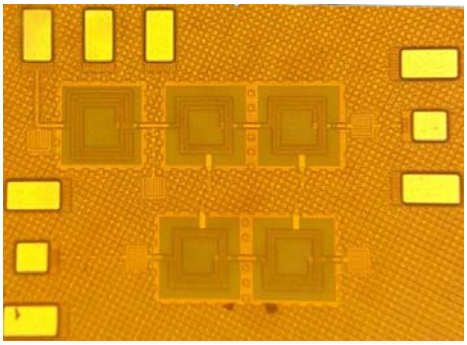
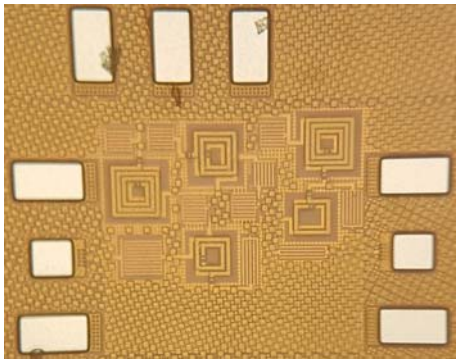


Fig. 9. Measurement results of the designed DAs.

setup. Broad bandwidth and high gain is obtained by using cascode structure and small area is obtained by using *m*-derived filter with stacked inductor in artificial transmission line. The 2-stage CSSDA shows peak S_{21} of 13 dB while the 2-stage DA exhibits peak S_{21} of 10 dB. Measured results show that the CSSDA provides higher gain than the DA while consuming less dc power.



(a) 2-stage DA (chip size: 720 × 540 μm2)



(b) 2-stage CSSDA (chip size: 580 × 450 μm2)

Fig. 10. Chip photograph.

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