Design of a low power 4th-order delta-sigma modulator with single reconfigurable amplifier

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***Abstract* - This paper describes the 4th-order feedback delta-sigma modulator with only one amplifier for the application of bio signal processing. The amplifier was reused 4 times by using time interleaving technique. For reducing KT/C noise which most related to integrating capacitance, first and second reused op-amp is designed to load 20pF integrating capacitor and third and fourth is designed to load 1pF and 250fF capacitor each. To solve stability issue made by different capacitance, this paper proposed stage variable op-amp. The modulator was designed with 0.18um CMOS standard process and dissipates the power of 354uW with supply voltage of 1.8V. The measurement results demonstrate the peak SNDR of 72.8dB and the ENOB of 11.8bits with an input signal frequency of 250Hz, a sampling frequency 256kHz, an input signal bandwidth of 1kHz, and an oversampling rate of 128. From measurement results FOM1 is calculated to 49.6pJ/step and FOM2 is calculated to 154.5dB.**

***Keywords*— 4th order feedback, Biological signal processing, Delta-Sigma modulator, Low power, Reconfigurable one operational amplifier**

I. INTRODUCTION

Recently, the demand for a low power and high resolution ADC (Analog to Digital Converter) has been increasing with the development of bio signal systems. A single block that consumes most of power in delta-sigma Modulator is OPAMP (Operational Amplifier). The first design technique is to employ two amplifiers using time-interleaving technique for 4th-order delta-sigma modulator [1]. Normally 4th-order delta-sigma modulators require four OP-AMPs. But using time-interleaving techniques and 4th-order delta–sigma modulators can be implemented with only two amplifiers. But this method has a disadvantage. Generally, the delta-sigma modulator increases the number of input capacitors due to the kT/C noise and reduces the number of back-end capacitors in order to decrease the chip size [10]. So using the same amplifier in both places is less efficient. The second design technique is a method of designing a delta-sigma modulator using an inverter instead of an operational amplifier [2-3]. This method can reduce the supply voltage and current by using inverters operating in the weak inversion region, which is easy to achieve low power. However, there is a drawback that it is difficult to achieve high resolution due to the low DC gain of the inverter. The third design technique time-interleaving technique and digital signal processing technique [4]. In the circuit proposed in [4], the first-stage integrator and the second-stage integrator are implemented with a single operational amplifier by operating the speed of the operational amplifier twice with the time-interleaving method, and the third-stage integrator is implemented by digital signal processing. This method achieved a low power consumption of 140uW and a high resolution of 14 bits or more. However, the 5-bit flash ADC is used as a quantizer for digital signal processing, which causes additional power consumption.

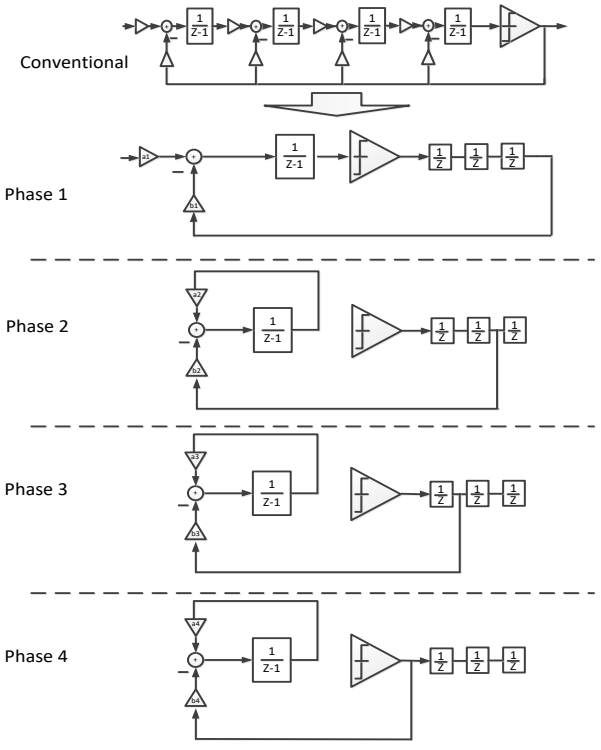

Fig. 1. Block diagram of the proposed fourth order feedback delta-sigma modulator with only one amplifier.

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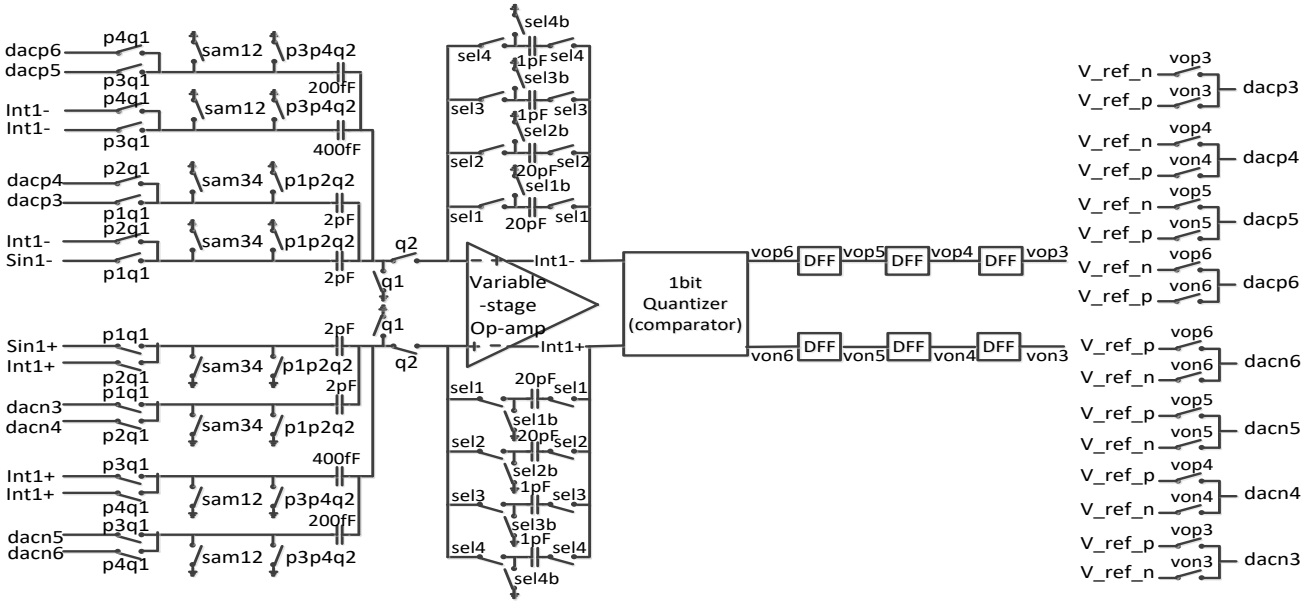

Fig. 2. Circuit diagram of the proposed low power 4th order modulator with reconfigurable op-amp.

In this proposal, using only one operational amplifier 4th-order delta-sigma modulator is described. This design is proposed to achieve a low power with reduced the number of op-amp and high resolution with 4th-order architecture. Second idea of the proposed design is putting reconfigurable operational amplifier. Conventional delta-sigma modulators suffer from kT/C noise and the noise is critical for the input-side only.

So the input capacitance is designed to be large for kT/C noise and the rest of the capacitance is designed to be small for chip size. Using only one amplifier generates a problem of phase margin.

To solve the problem Reconfigurable amplifier is used. This paper is organized as follows. In section II, the design technique of the fourth order modulator with Reconfigurable op-amp will be described. The measurement results are discussed in section III and conclusions are drawn in section IV.

II. THE PROPOSED ARCHITECTURE

TABLE 1. Coefficients of the loop factor

Coefficient	Value	Coefficient	Value
a1	0.1	b1	0.1
a2	0.1	b2	0.1
a3	0.4	b3	0.2
a4	0.4	b4	0.2

TABLE 2. Correlation between Coefficient and Capacitor

Coefficient	Value	Coefficient	Value
a1	Cs1/Ci1	b1	Cf1/Ci1
a2	Cs1/Ci2	b2	Cf1/Ci2
a3	Cs2/Ci3	b3	Cf2/Ci3
a4	Cs2/Ci4	b4	Cf2/Ci4

The block diagram of the proposed architecture is presented in Fig.1. It employs the fully differential fourth order feedback architecture with only one amplifier. The conventional fourth order feedback delta-sigma modulator requires four op-amp, but proposed modulator requires only one. It reduces power dissipation to one-quarter.

Fig. 1 shows four phases of proposed delta-sigma modulator. In each phase, the delta-sigma modulator operates as each stage of a conventional delta-sigma modulator. So, four times faster than a conventional delta-sigma modulator is required in sampling frequency. This architecture employs reconfigurable circuit topology with time interleaving technique.

During the first phase (Phase 1) in Fig. 1, the modulator performs the sampling and integration. The second phase (Phase 2) in Fig.1, the modulator performs the sampling and integration with the output signal of the op-amp in Phase 1. The third phase (Phase 3) in Fig. 1, the modulator performs the sampling and integration with the output signal of the op-amp in Phase 2. The fourth phase (Phase 4) in Fig. 1, the modulator performs the sampling and integration with the output signal of the op-amp in Phase 3.

From the structure, the NTF is obtained as follows, and the coefficients of each stage are shown in Table 1, Table 2 shows the correlation between coefficient and capacitor and Table 3 shows the physical value of capacitors within each integrator in terms of the unit capacitor, Cu1 and Cu2. Cu1 is 250fF and Cu2 is 50fF.

$$NTF(z) = \frac{(z-1)^4}{z^4 + C_3 z^3 + C_2 z^2 + C_1 z + C_0} \quad (1)$$

$$C_0 = a_4 b_3 - b_4 - a_3 a_4 b_2 - a_2 a_3 a_4 b_1 + 1 \quad (2)$$

$$C_1 = 3b_4 - 2a_4 b_3 + a_3 a_4 b_2 - 4 \quad (3)$$

$$C_2 = 6 + a_4 b_3 - 3b_4 \quad (4)$$

$$C_3 = b_4 - 4 \quad (5)$$

Circuit schematic of the proposed low power 4th order ΣΔ modulator with only one amplifier is presented in fig. 2. The value of all the capacitors associated with those coefficients is illustrated in Fig. 2. In the clock phase 1, the switches of p1q1, q1, sam12 are turned on for half a period, the signals are sampled, the switches of p1p2q2, q2, sel1 are turned on for the remaining half period, and the integration operation is performed. In the clock phase 2, the switches of p2q1, q1, sam12 are turned on for half a period, the output signal of the first integrator is sampled again, and the switches p1p2q2, q2, sel2 are turned on for the remaining half period to perform the integral operation. In clock phase 3, the switches of p3q1, q1, and sam34 are turned on for half a period, the output signal of the second integrator is sampled again, and the switches of p3p4q2, q2, and sel3 are turned on for the remaining half period. In clock phase 4, the switches of p4q1, q1, and sam34 are turned on for half a period, the output signal of the third integrator is sampled again, and the switches of p3p4q2, q2, and sel4 are turned on for the remaining half period.

TABLE 3. The physical value of capacitors within each integrator in terms of the unit capacitor, Cu1 and Cu2

Capacitor	Value	Capacitor	Value
Cs1/Cu1	8	Ci1/Cu1	80
Cs2/Cu2	8	Ci2/Cu1	80
Cf1/Cu1	8	Ci3/Cu1	4
Cf2/Cu2	4	Ci4/Cu1	4

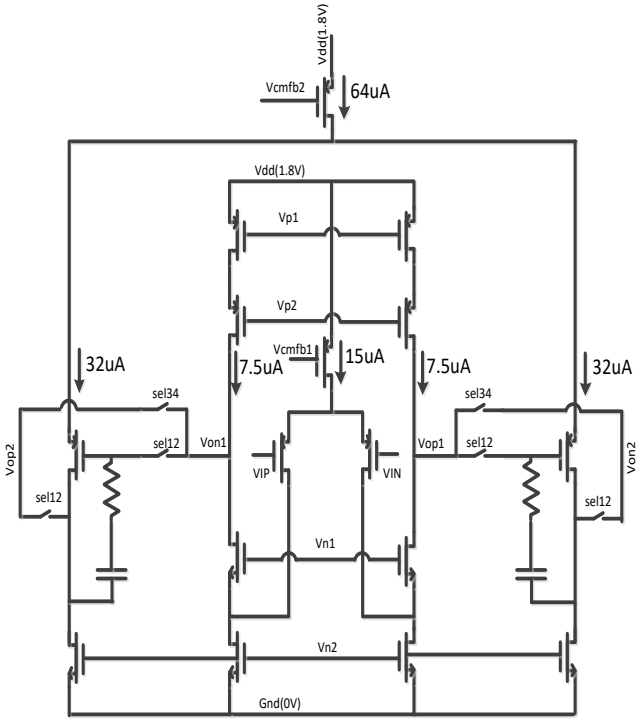

Fig. 3. Circuit schematic of the used Reconfigurable Operational Amplifier

The phase diagram of the clock signals is demonstrated in Fig. 4. All of the clock signal are non-overlapping clock because of using switched capacitor circuits stable and proper. The non-overlapping clock circuit can prevent signal interference between the sampling and integration operations when the signal passes through the dswitch-capacitor circuit. Also, since the time division technique is used, a variety of complicated clock signals are required in the proposed structure. First, the signals of q1, q2, q1d and q2d are required in the general structure. And q1d and q2d represent delay signals of q1 and q2, respectively. The q1 is the sampling mode and the q2 is the integration mode. The basic clock signals q1 and q2 are generated first, and q1 and q2 are used as references to generate p1q1d, p2q1d, p3q1d, p4q1d, p1q2d, p2q2d, p3q2d and p4q2d. Next, the clock signals p1~, p2~ are referenced to generate clock signals required for the circuit using digital logic.

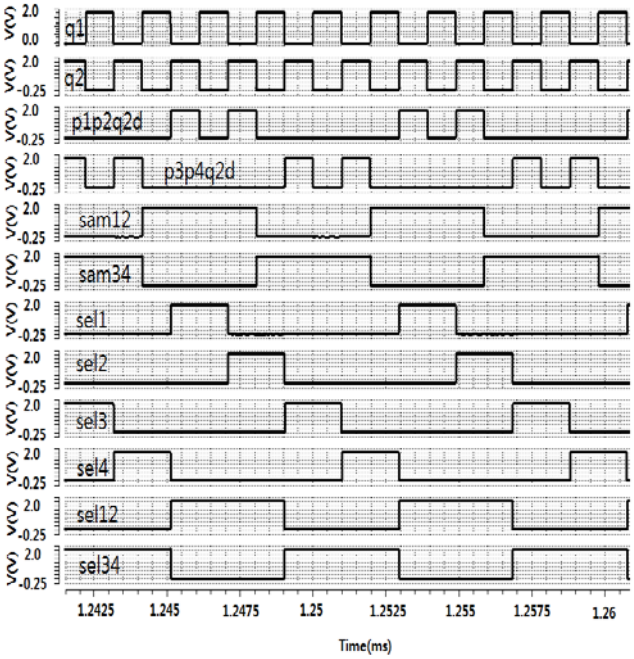

Fig. 4. Phase diagram of the clock signals to control both sample mode and integration mode.

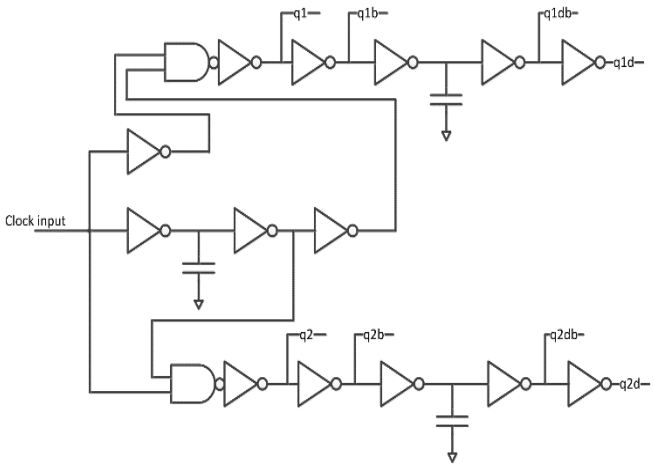

Fig. 5. Circuit schematic of non-overlapping clock generator

The Circuit schematic of the used stage-variable op-amp is presented in Fig. 3. Conventional Delta-sigma Modulator suffers from kT/C noise and the noise is critical for the input-side only. So the input capacitance is designed to be large and the rest of the capacitance is designed to be small. The designed sampling capacitance of the first and second phase is 2pF. The designed integration capacitance of the first and second phase is 20pF. And the designed sampling capacitance of the third and fourth phase is 400fF. The designed integration capacitance of the third and fourth phase is 1pF. Using only one amplifier for 4th order Delta-Sigma Modulator generates a problem of phase margin because of the capacitance difference. In order to operate safely, Phase margin of the modulator must be in the 60 to 90 degrees [5].

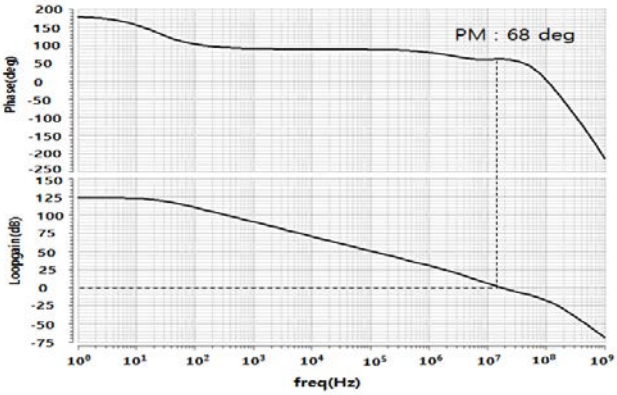

Fig. 6. SPICE simulation of the OP-amp in phase 1 and 2

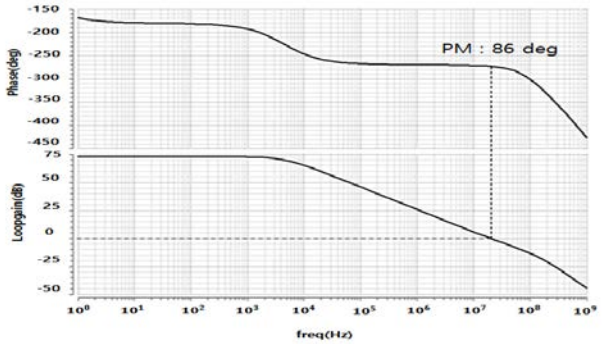

Fig. 7. SPICE simulation of the OP-amp in phase 3 and 4

If the phase margin exceeds 90 degrees, the integration speed is slow and there is a risk that the integration cannot be performed within the integration time.

Because of the on-resistance of the switch, zero occurs in the switched-capacitor integrator. Because of the large capacitance in the first and second stages, the problem is that zero enters deep into gain bandwidth of the op-amp. So the phase margin goes over 90 degrees, which slows the integrator. Equation (6) shows zero occurring in the integrator loop [11]. The on-resistance of the switch used in the circuit is 812Ω and the calculated zero is 19.6MHz.

$$f_z = \frac{1}{2\pi 3R_{on}[(C_s+C_f)||C_i]} \quad (6)$$

To solve the problem, Reconfigurable amplifier is used. In the first and second Phase, the reconfigurable amplifier operates as a 2-stage. In the third and fourth Phase, the reconfigurable amplifier operates as a 1-stage. Based on folded cascade structure, loop gain of the op-amp in the first and second phase is 125dB, phase margin is 68deg and unity gain frequency is 17MHz. The loop gain of the op-amp in the third and fourth phase is 75dB, phase margin is 86deg and unity gain frequency is 19MHz. So the op-amp operates safely in all phase. The spice simulations of the OP-amp are presented in Fig. 7.

The proposed delta-sigma modulator is designed with a 0.18um CMOS process and the layout of the designed circuit is represented in Fig. 8 occupied a core area of 800μm x 900μm. The layout area of one amplifier and Gm bias is 300μm x 70μm. This area is about 3% of the total area. Because the area of the capacitor is so large, reducing the number of amplifiers has little effect on area reduction.

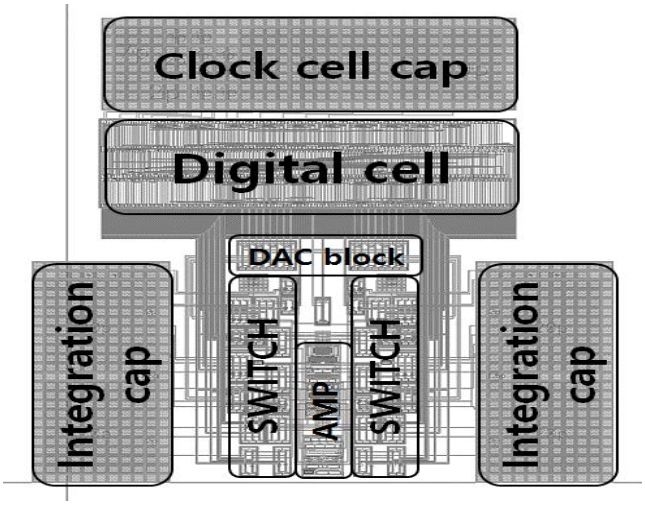

Fig. 8. The layout of proposed delta-sigma modulator

Fig. 9 Shows the FFT simulation results of the proposed delta-sigma modulator. The FFT simulated results demonstrate SNR of 80.62 dB, ENOB of 13.1bits and power dissipation of 352uW at sampling frequency of 128kHz, input signal frequency of 250Hz, and the magnitude of the input signal, Vdd/2.

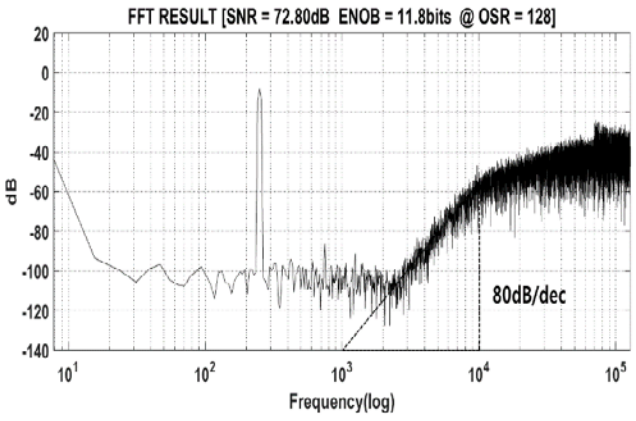

Fig. 9. Measured modulator output FFT result.

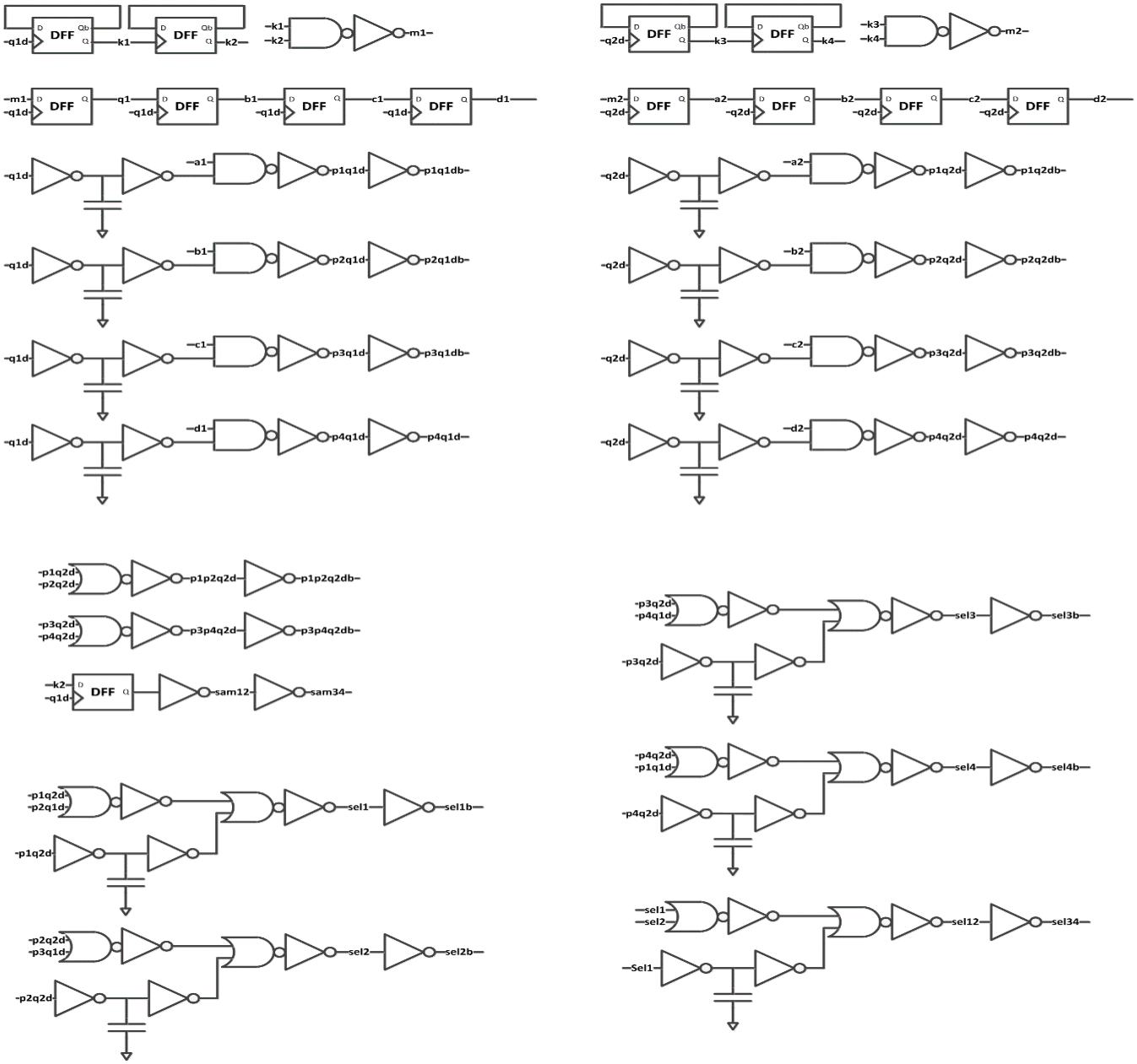

Fig. 10.clock signal modulator

III. RESULTS AND DISCUSSION

The simulation of the designed modulator was performed using CMOS 0.18um 1 poly 6 metal process library. The tools used were spectre and hspice and FFT was performed using spectra's own spectrum analysis function. The number of samples of the bitstream is 4096, and the FFT is performed by suppressing the signal leakage through the hanning window. For the OSR 128, the operating clock frequency is 1.024MHz so that the sampling clock frequency is 256kHz The simulation was performed by 900mVpp input sine wave at a frequency of 250Hz. The simulation results show that SNDR is 80.64dB and ENOB is 13.1bit.

The maximum SNDR and DR were obtained by varying the amplitude of the input signal by applying a 250Hz input sine signal at 256kHz sampling clock frequency. Fig.10. Shows the output signal FFT results at 131072 bit stream samples at 804mVpp.

The measurement results demonstrate the peak SNDR of 72.8dB and the ENOB of 11.8bits. As shown in the graph, the degree of noise shaping is 40dB due to the kT/C noise, but when the slope of the tangent line is plotted, it can be confirmed that it is 80dB/decade. The power consumption was measured as 354μW with an analog current of 165.9μA and a digital current of 31μA. Analog current is Gm bias current: 64.17μA, Op-amp current: 96.93μA, Comparator current: 6.89μA, digital current is consumed in the clock generator and buffer. Power consumption can be reduced by 25% compared to a conventional structure using four amplifiers.

Fig.11. shows the result of SNDR measurement according to input signal size, where DR was measured at 90dB. Table 4 shows the result of ENOB for each frequency. Table 4. Compares the performance of the proposed modulator with

the performance of other papers. The Walden and Schreier FOM (figure of merit) to express the performance of the delta-sigma modulator is shown in equation (7) and (8).

TABLE 4. ENOB for each frequency

Frequency	ENOB
1kHz	11.3
500Hz	11.4
250Hz	11.8
125Hz	11.9
62.5Hz	11.8
31.25Hz	11.9

The proposed circuit shows that the power consumption, FOM(Walden) is reduced to about half and the FOM (Schreier) is increased by 12dB compared with the paper [4] which implements the fourth order with two operational amplifiers. Compared with the inverter-based paper [2], the power consumption increased somewhat, but the signal-to-noise ratio increased by 8dB and DR increased by 15dB. Compared to the other inverter-based paper [16], DR is increased by 10dB and it can be seen that power consumption is greatly reduced.

$$\text{FOM(Walden)} = \frac{P}{2^{ENOB} \times 2 \times BW} \quad (7)$$

$$\text{FOM(Schreier)} = \text{DR} + 10\log\left(\frac{\text{BW}}{\text{P}}\right) \quad (8)$$

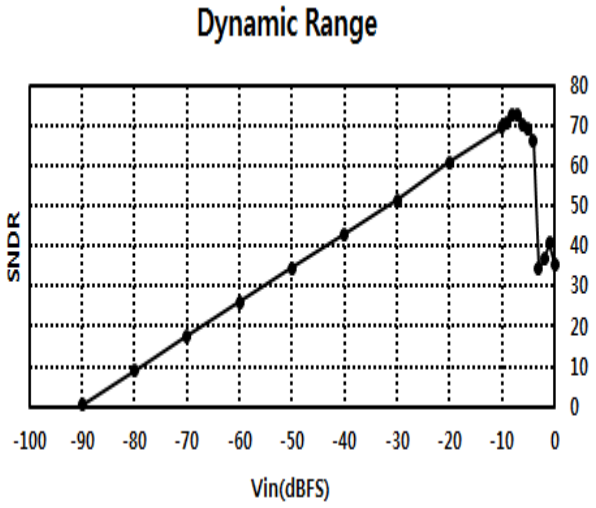

Fig. 11. Measured result of SNDR versus input signal amplitude.

IV. CONCLUSIONS

In this paper, a low power, high resolution 4th-order delta-sigma modulator for biological signal processing is designed. The proposed 4th-order delta-sigma modulator reduces the number of operational amplifiers from four to one using time division techniques for low power. In addition, the amplifier is designed to vary in stages according to the capacitor value in order to stably drive the input and back-end capacitors of the modulator with large size difference considering kT/C noise and chip size. In order to satisfy the resolution of 12 bits or more in the OSR, a 4th-order delta-sigma modulator structure is used and a 1-bit feedback structure is designed.

The proposed 4th-order delta-sigma modulator was fabricated using 0.18μm CMOS n-well 1 poly 6 metal process. The measured results show that the power consumption of 354μW at a supply voltage of 1.8V and the operating frequency of 256kHz and OSR of 128 times when the input signal of 250Hz was applied. The maximum SNDR was 72.8dB and the ENOB was 11.8bit. From the results, FOM(Walden) was calculated as 49.6pJ/step and FOM(Schreier) was calculated as 154.5dB.

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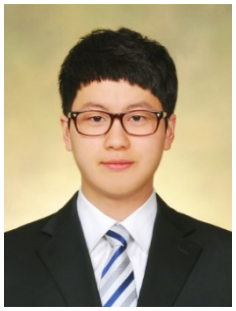

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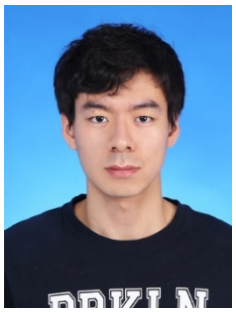

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